FSU CAPS
Overview and Updates

October 2024

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FSU Center for Advanced Power Systems

Collaborations with Academia and National Labs

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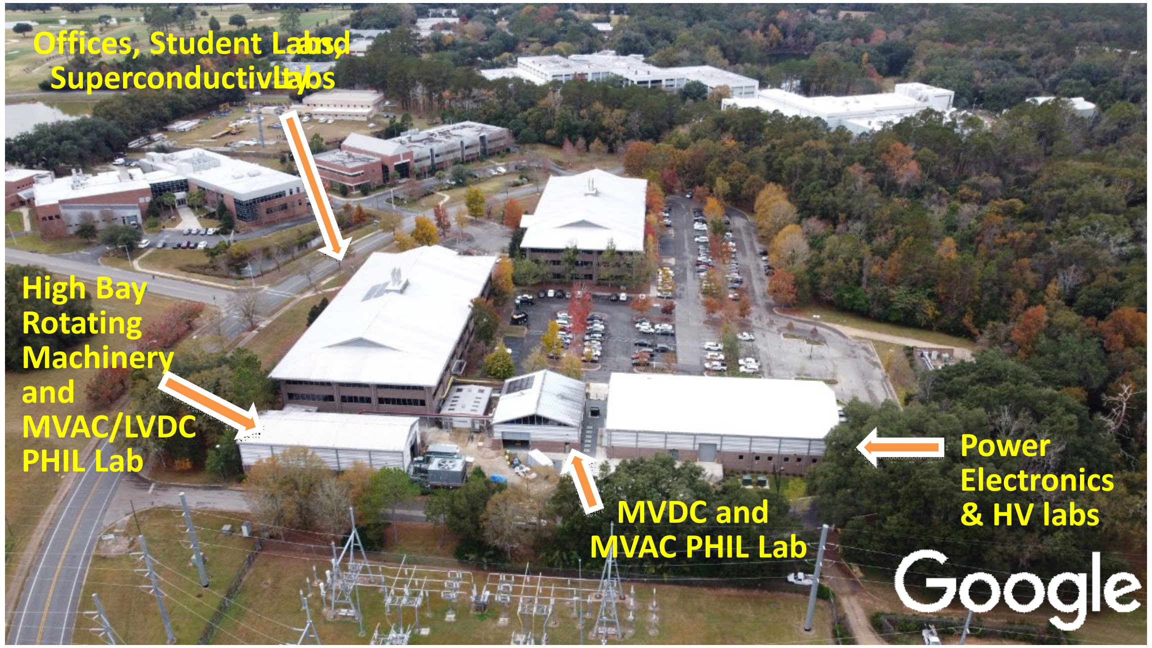
University of South Carolina
Johns Hopkins Applied Physics Laboratory
National High Magnetic Field Laboratory
Massachusetts Institute of Technology
U.S. Naval Academy
Purdue University
INL Idaho National Laboratory
Clarkson
Virginia Tech
Electric Ship Research and Development Consortium (ESRDC)
The University of Queensland Australia
KIT Karlsruhe Institute of Technology
The University of Texas at Austin
University of Wisconsin–Milwaukee (UWM)
University of Texas Arlington
Mississippi State University
fh Oberösterreich University of Applied Sciences Upper Austria



Industry Collaborator and Sponsors

arpa-e CHANGING WHAT'S POSSIBLE
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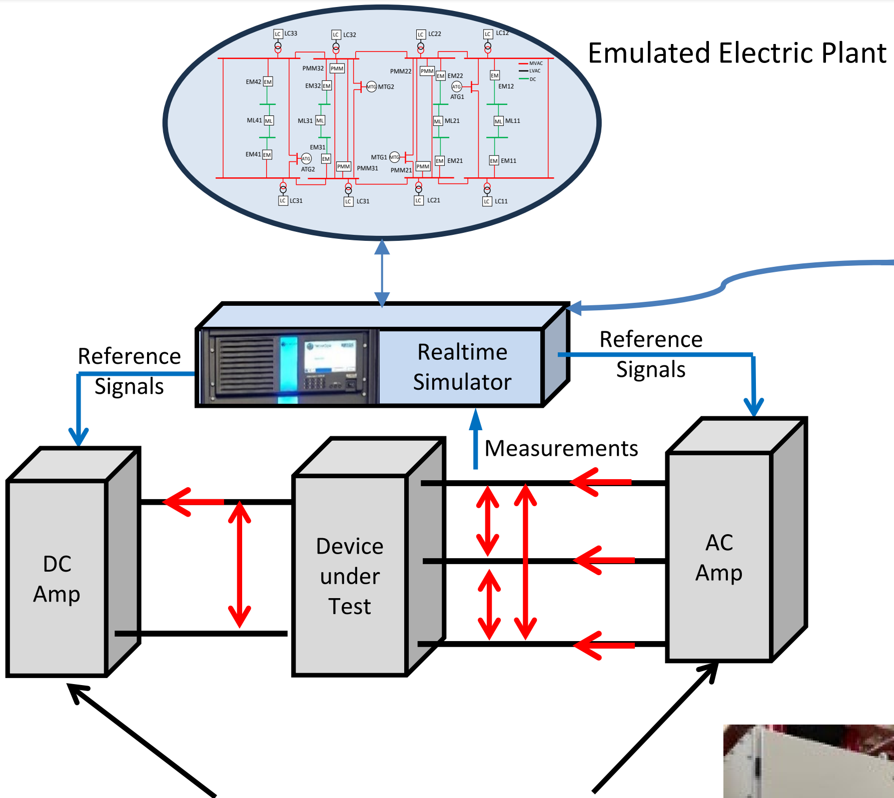
Power Hardware-in-the-Loop (PHIL) Simulation

Create a Virtual yet Realistic Environment to Rapidly Test Equipment and Interfaces: PHIL

- Couple Device Under test (DUT) to a Real Time Computer Simulation using amplifiers and/or actuators (preserves natural coupling)

- Use of PHIL Simulation
  - Testing in Realistic Environment
  - Early integration testing
  - Flexibility to quickly change surrounding system and conditions to test equipment performance envelope
  - Validate System Specification & Interfaces
  - Testing with yet unrealized system
  - Test extreme conditions within controllable lab environment



CAPS RT Simulators
- RTDS Novacore (9)
- SpeedGoat (2)
- Typhoon HIL (3)
- Opal-RT (2)

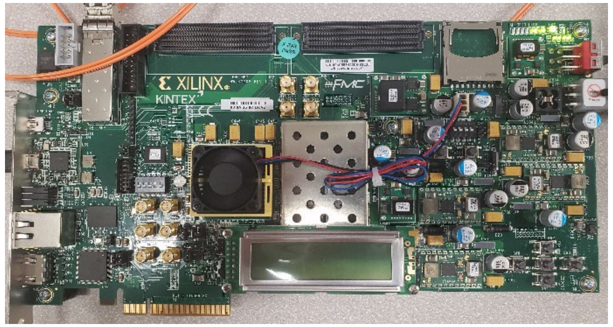
Variable Voltage Source

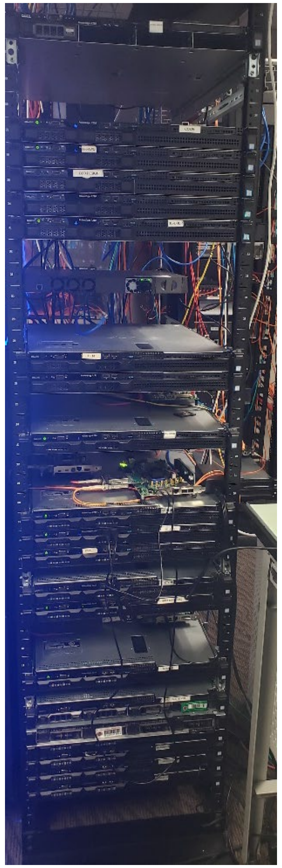
Optimus Power Units (2)

Co-Simulation

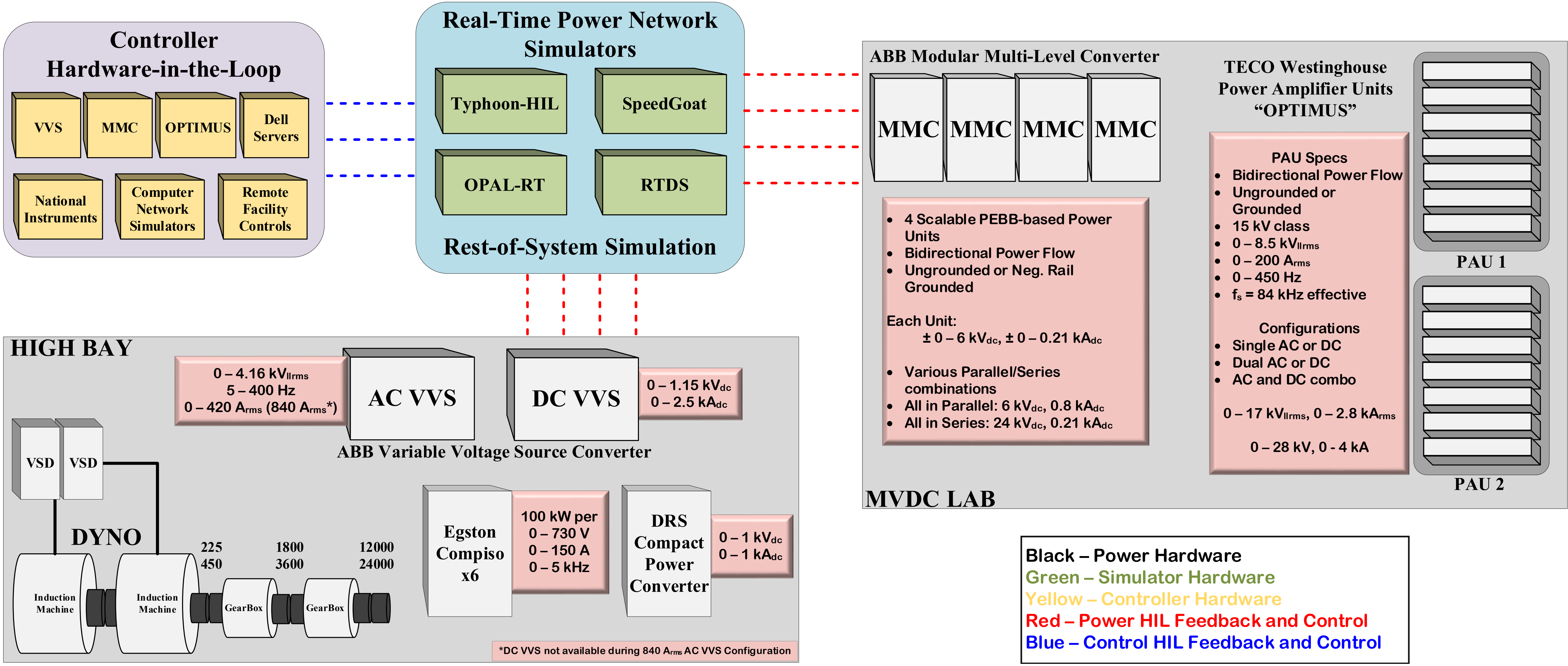
- Portion of model on real-time simulator (RTS) and portion of model on co-simulation machines
- Model on co-sim machine executes faster than real time – clocked from RTS
- Model on co-sim machine can execute in native software package (e.g. MATLAB/Simulink, nVe, compiled executable, etc.)
- Useful for
  - Protected vendor models that cannot be ported or re-compiled for RTS as target
  - Complicated models that are difficult to manually port
  - Models with subsystems allowing larger time-step sizes (e.g. generator set with prime mover, AVR/exciter, and synchronous machine)
  - Controls
- FPGAs used for high-speed digital link between co-sim machine and RTS

- RTDS 9x 10-NovaCors
- (35) x86-64 servers
- (30) Xilinx-based FPGA





5 MW PHIL Facility Overview



Michael “Mischa” Steurer pioneered HIL and initiated IEEE WG P2004.

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- Secretary: **Blake Lundstrom**
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  Enphase Energy, Fremont, CA, USA
- Sponsor: **PELS,** Co-sponsor: **IAS, IES**
- Collaboration**: PSRC WG CTF-33**; IEEE task force (TF) on “Real-Time Simulation of Power and Energy Systems”, chaired by Dr. Omar Faruque, under **IEEE WG 15.08.09** (within the General System Subcommittee of the IEEE PES T&D Committee)

Generator Testing – Constant Power

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Generator Testing Motivation

Improve (cost) efficiency of backup generation

- Re-rate and save on units required
- Hardware of interest: diesel generator (DG) with 13.8 kV, 60 Hz, 3.5 MVA

Testing DG with increased generation capacity at increased power factor

- 2.8 MW @ 0.8 p → 3 MW @ 0.98 pf

Factory Acceptance Test (FAT) shows DG able to handle 0-100% block loads w/ load bank

- FAT with load banks not reflecting application load:
- Feasible for constant power loading?
  - First of its kind: generator + PHIL constant power load

Real-time Simulator


Load banks

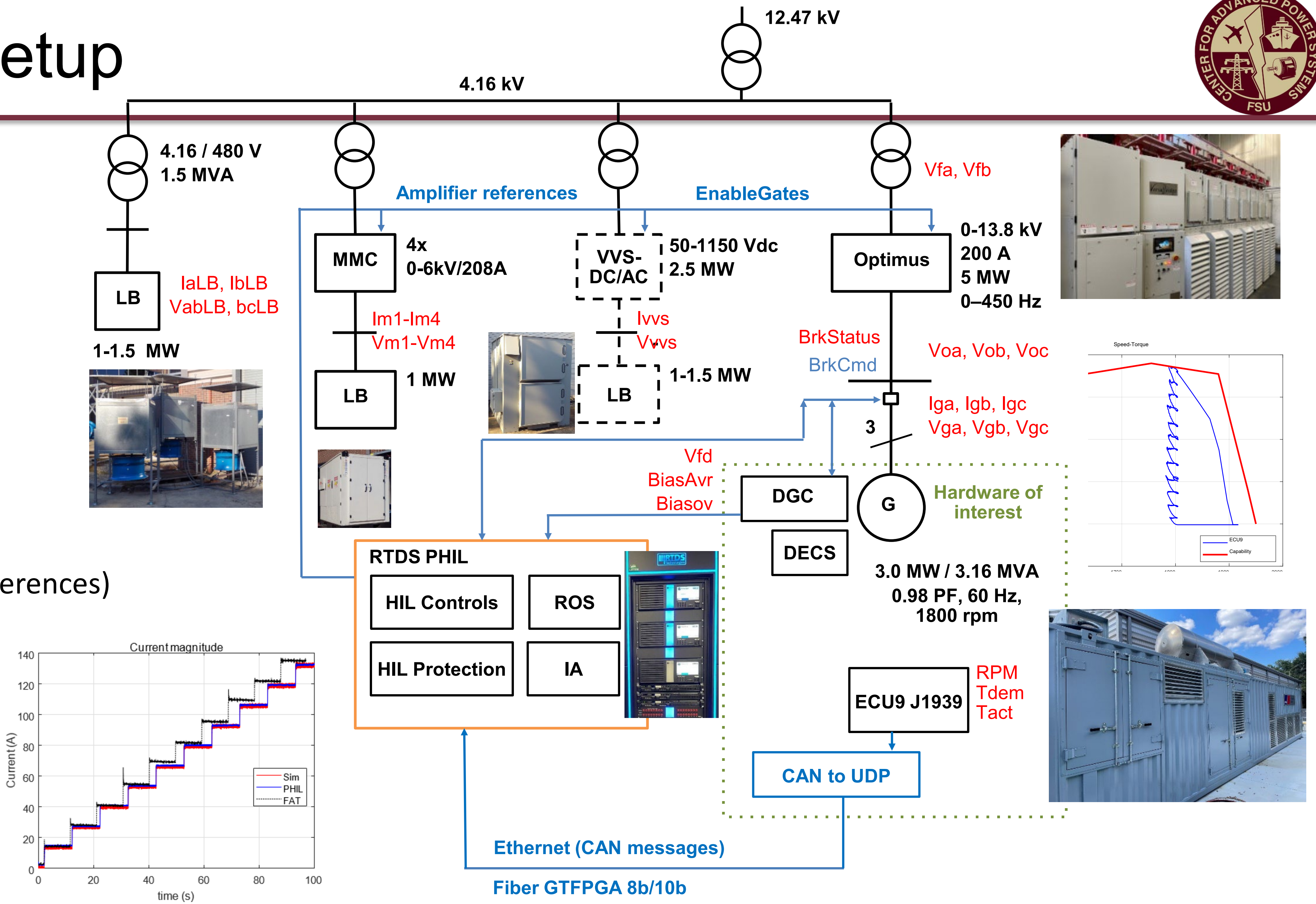
PHIL Setup

Hardware components
- 1x Generator under test

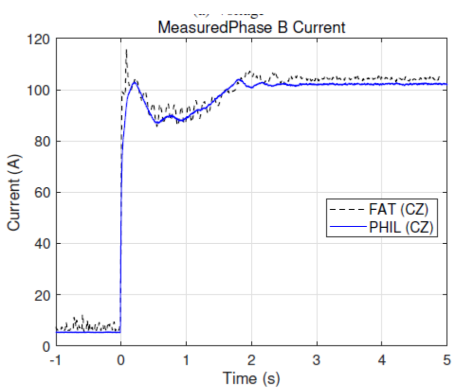
Test infrastructure
- Power amplifiers
- Load banks

Instrumentation
Signals to RTS (in red)

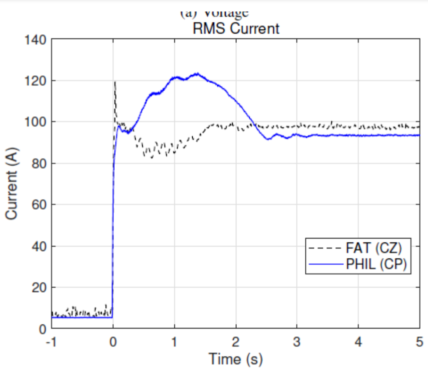
Communication (in blue)
- From RTS to amplifiers (references)
- CANbus

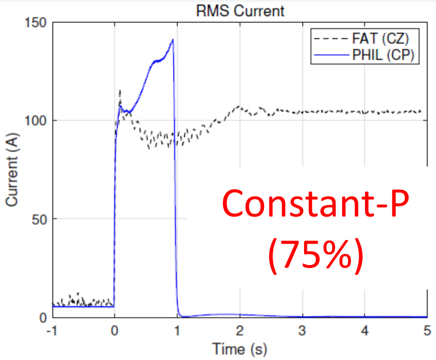


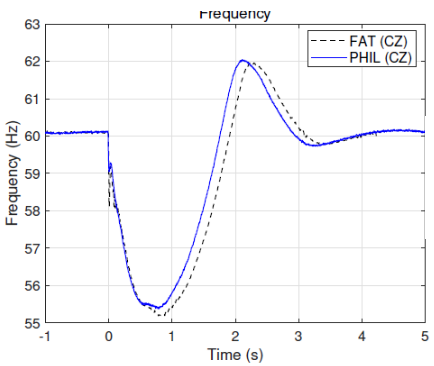
3 MW, 13.8 kV Diesel Generator Set



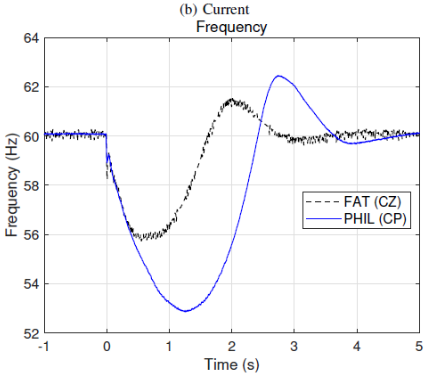
Constant-Z
(75%)

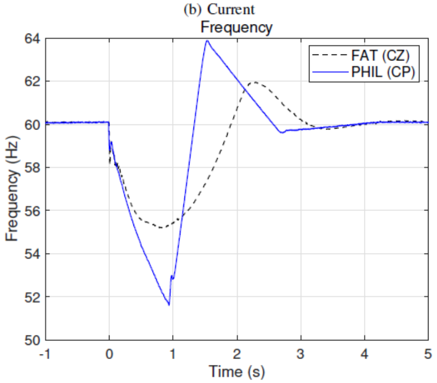




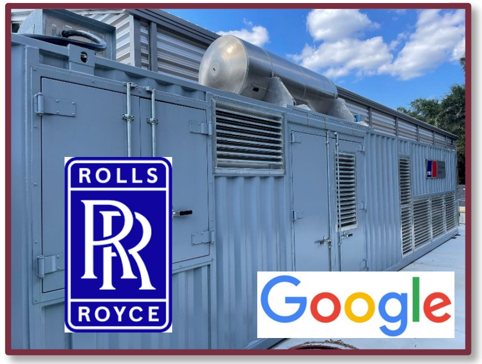


Constant-P
(70%)

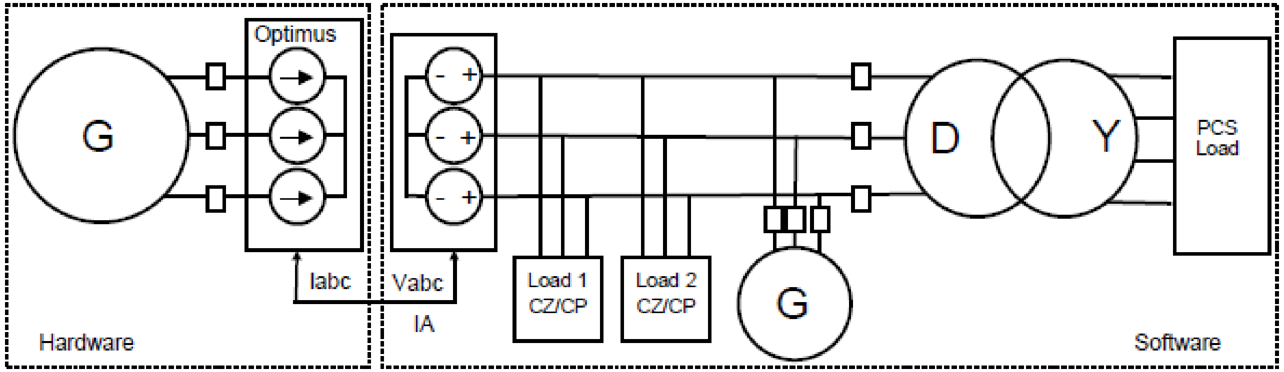




- Tested 3 MW, 13.8 kV DG
- PHIL Interface
  - DQ-frame DIM IA
  - Optimus amplifier configured for 13.8 kV AC, current control mode
- Studied response to dynamic changes in constant-power loads
  - Generator handled 100% constant-Z load step
  - Generator could only handle 70% constant-P load step
  - Experiment gracefully shut down without tripping the generator



13.8 kV, 3 MW DG



Schoder, K., et al. "Dynamic Load Testing of a Diesel Generator Using Power Hardware-in-the-Loop Simulation." *2023 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2023.

Virtual DIM

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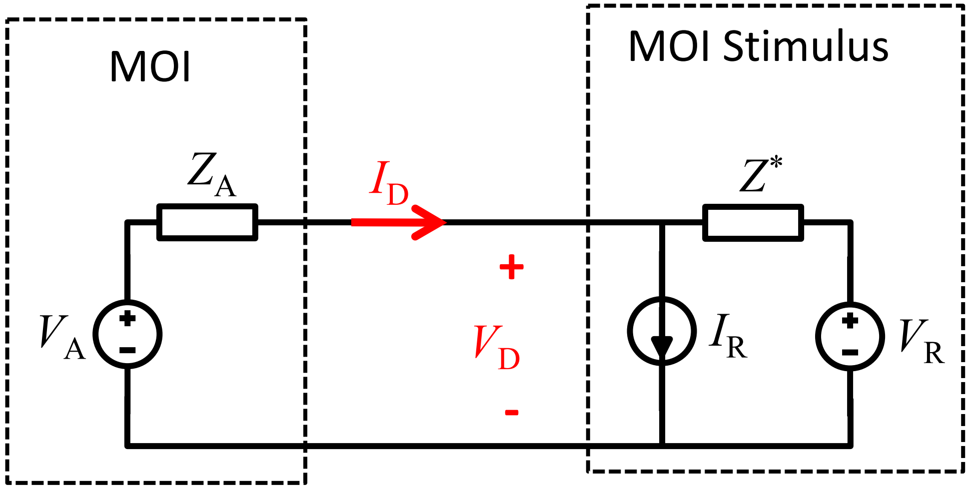
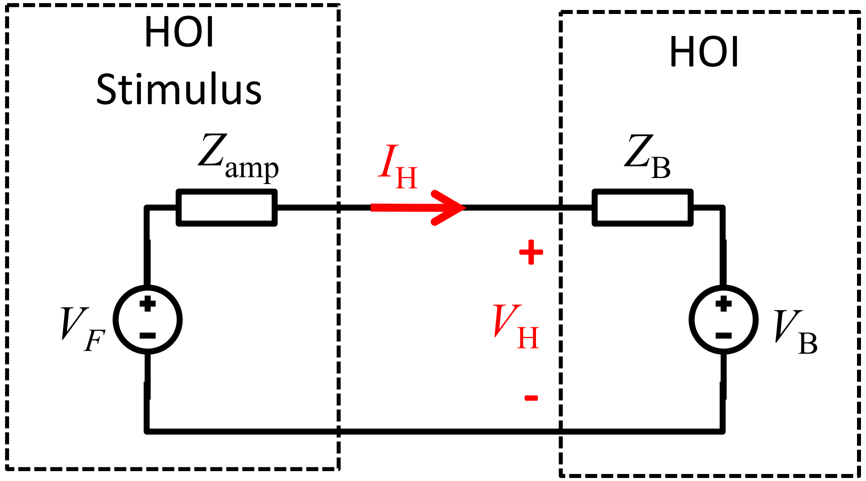
Damping Impedance Method

- Damping Impedance Method (DIM) interface approach (IA) commonly used in cases in which the ITM IA may not be stable
- If the damping impedance is closely matched to the HOI impedance
  - Guarantees stability
  - Generally shows high accuracy
- Potential issue with DIM IA if the HOI impedance is not easily represented by passive network (e.g. power converters in the low frequency range)
- Virtual DIM offers more flexibility – modeling arbitrary transfer function
  - Delays may affect representation of damping impedance at higher frequency
- Partial Virtual DIM combines flexibility of virtual DIM with better representation of damping impedance in the high frequency range

Will be presented at IECON'2024.

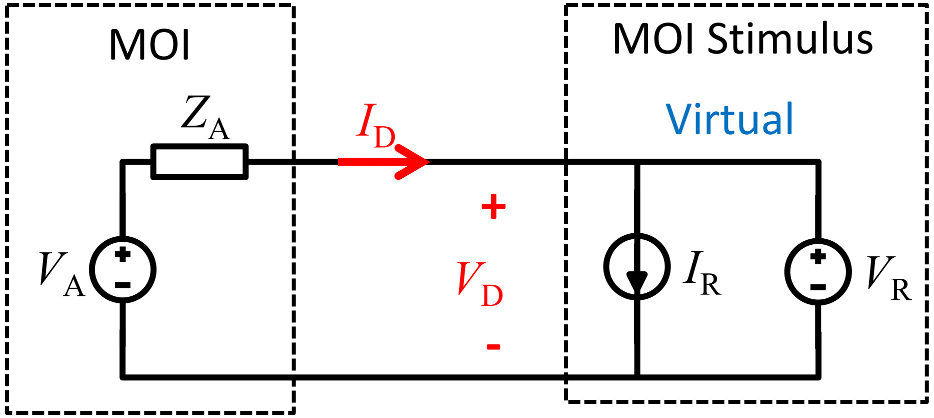


$I_{R-ref} = I_H \quad V_{R-ref} = V_H$

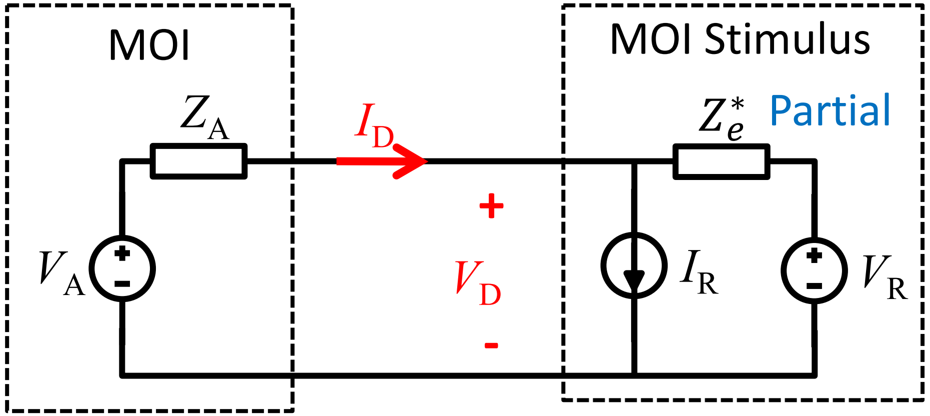


$V_{F-ref} = V_D$

Virtual Damping Impedance Method

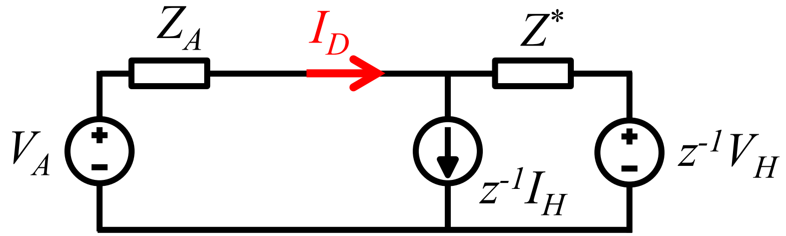


$$I_{R-ref} = I_H$$
$$V_{R-ref} = V_H - (I_D - I_H)Z^*$$

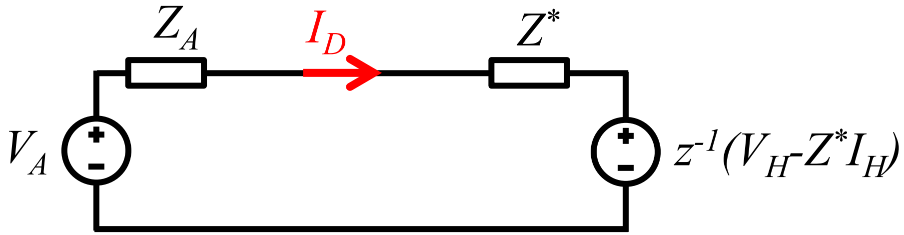


$$I_{R-ref} = I_H$$
$$V_{R-ref} = V_H - (I_D - I_H)Z_v^*$$

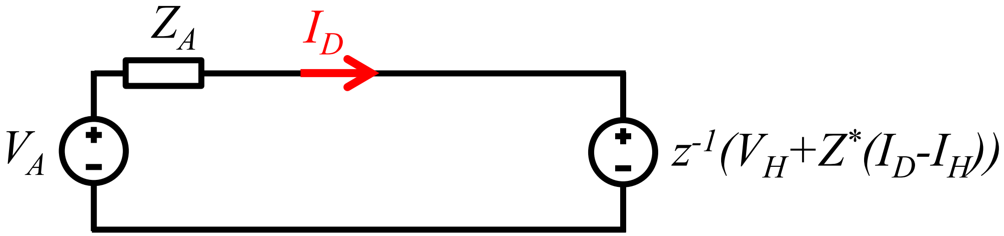
DIM with Explicit Damping Impedance (Normal)



DIM with Explicit Damping Impedance (Thevenin Equivalent)



DIM with Virtual Damping Impedance



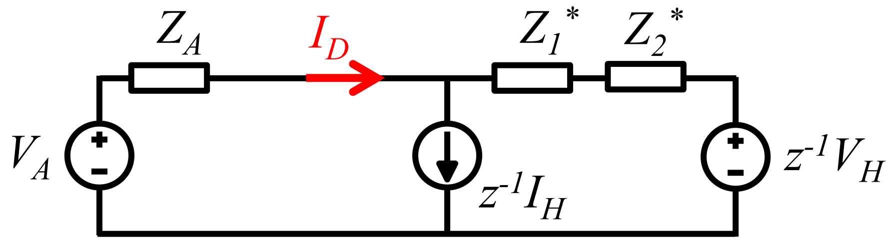
Consider Partial Virtual Impedance

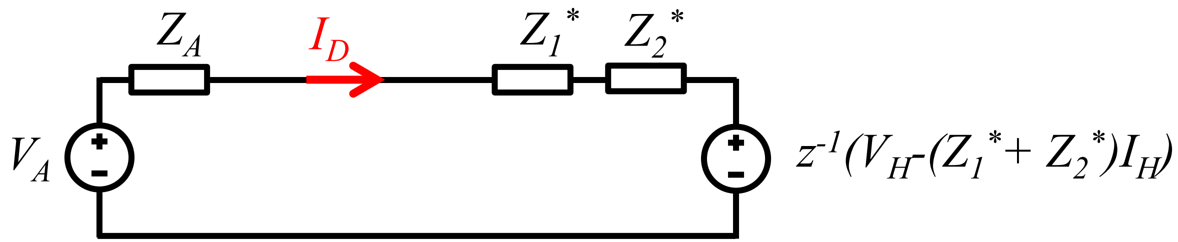
Application that benefits is to explicitly represent **high frequency portion of impedance** (which may well be represented by a passive network)

…along with a **low-frequency MOI injection model**, which may represent control behavior and not be well modeled by a passive network.

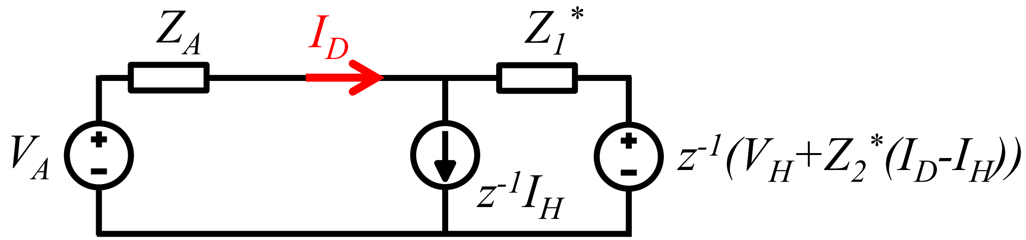
Partition Z* into two components where, for example, Z_1* captures high frequency behavior and Z_2* captures low frequency behavior.

$$Z^*=Z_1^*+Z_2^*$$



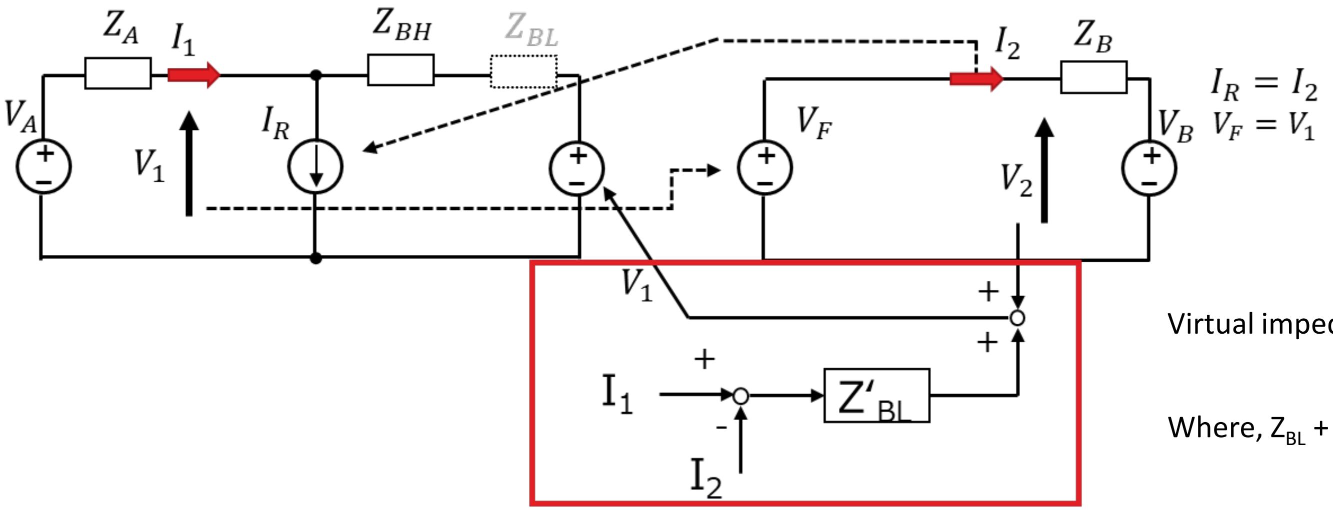


DIM with Partial Virtual Damping Impedance



PV-DIM

This method separates explicit impedance and ideal impedance.
It possess high stability and ease to introduce impedance characteristic.



Virtual impedance : Z'_B

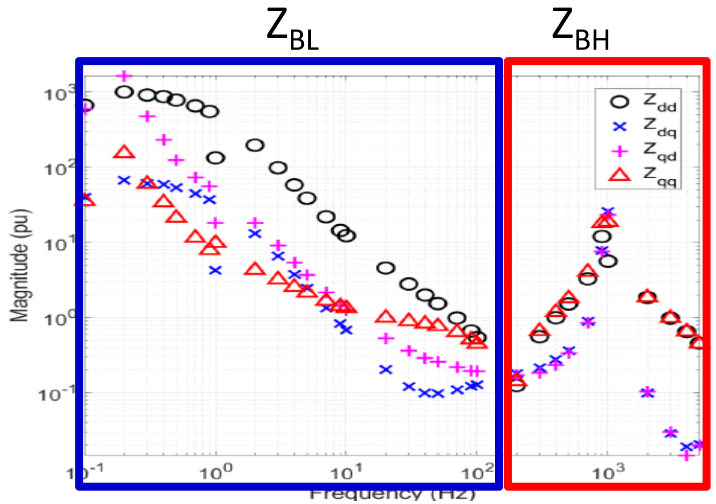
Where, $Z_{BL} + Z_{BH} = Z_B$

V-DIM open-loop gain

$$\frac{e^{-s2T_d}Z_B^*}{Z_A}$$

PV-DIM open-loop gain

$$\frac{e^{-s2T_d}Z_{BL}^*}{(Z_A+Z_{BH})}$$



Z_{BL} : low-band frequency

Z_{BH} : high-band frequency

Multi-Phase Linear Analysis

October 2024

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Motivation

Generalized linear analysis of interface algorithms for multi-phase applications.

- Current practices
  - Custom analysis specific to the case study and PHIL Interface Algorithm (IA)
  - Conduct multi-phase PHIL without proper assessment of stability, accuracy and sensitivity
- Application and analysis of PHIL experiments utilizing linear analysis framework has been conducted for single phase interface system[1] but not for multi-phase systems
- Builds on Extended Lawrence Architecture (ELA) framework
- Useful framework applicable to PHIL experiments independent of IA
  - Successfully applied to a project

[1]. James Langston, "APPLICATION AND ANALYSIS OF THE EXTENDED LAWRENCE TELEOPERATION ARCHITECTURE TO POWER HARDWARE-IN-THE-LOOP SIMULATION" PhD dissertation, FSU 2018.

Current Multi-Phase PHIL Analysis Methodology

- No common framework for analyzing different IA for a given PHIL experiment[4]
- Hence deriving expressions and analyzing stability, accuracy and sensitivity limited to specific experiment being conducted

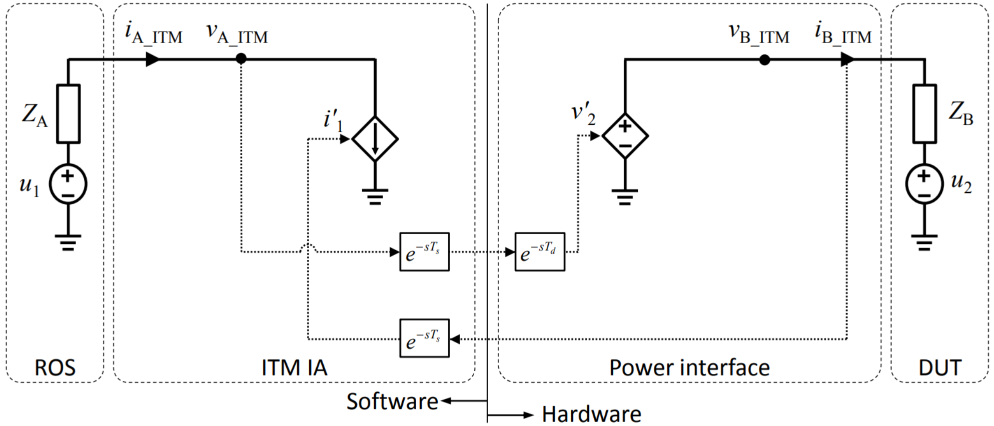


Fig. 3 PHIL system with ITM IA

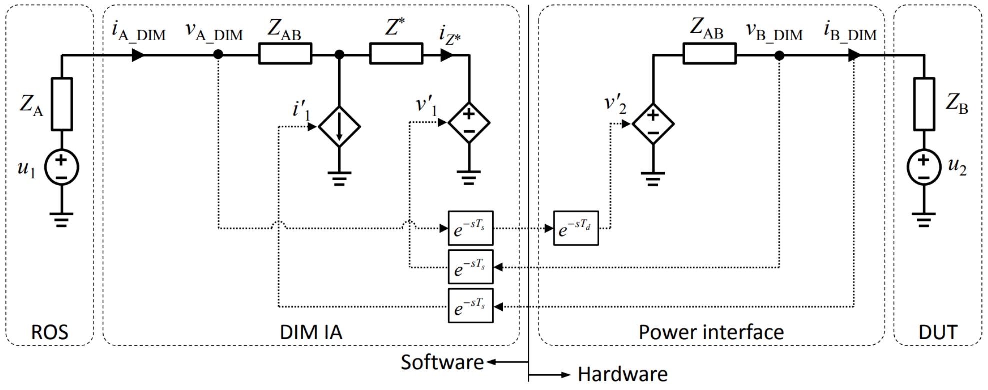


Fig. 5 PHIL system with DIM IA

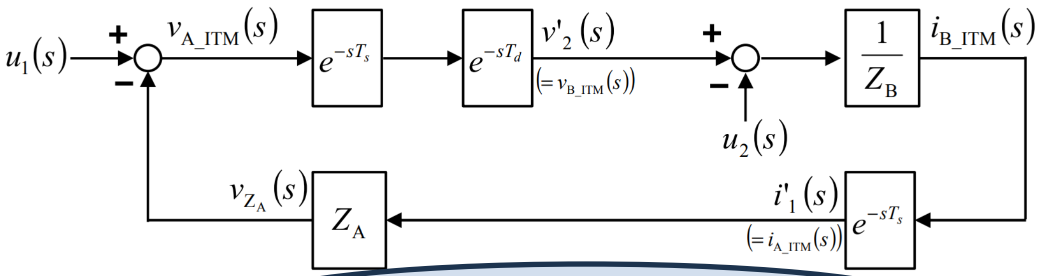


Fig. 4 Equivalent block diagram of the PHIL system with ITM IA

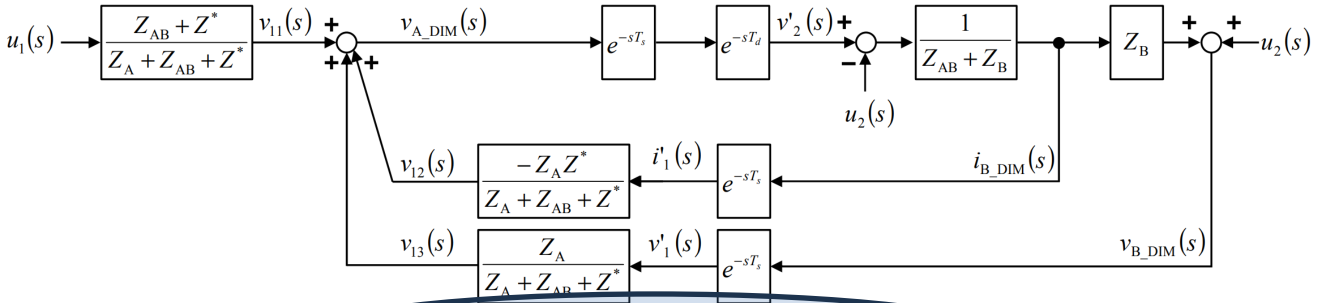
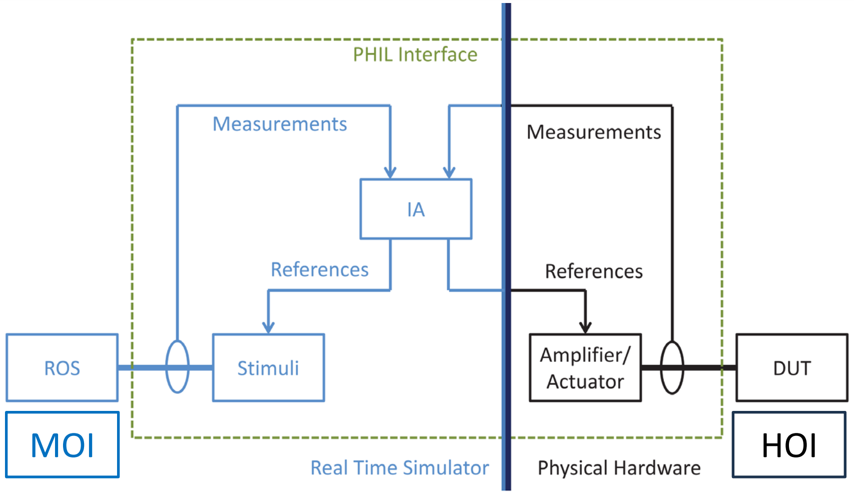


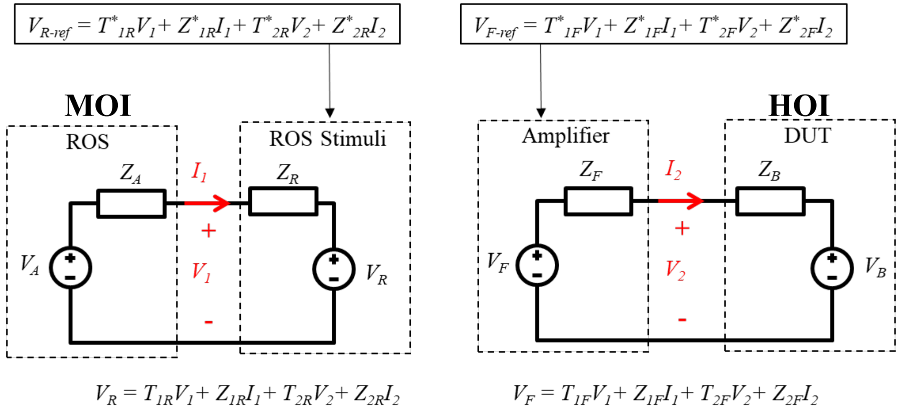
Fig. 6 Equivalent block diagram of the PHIL system with DIM IA

[4]. T. Hatakeyama, A. Riccobono and A. Monti, "Stability and accuracy analysis of power hardware in the loop system with different interface algorithms," *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, Norway, 2016

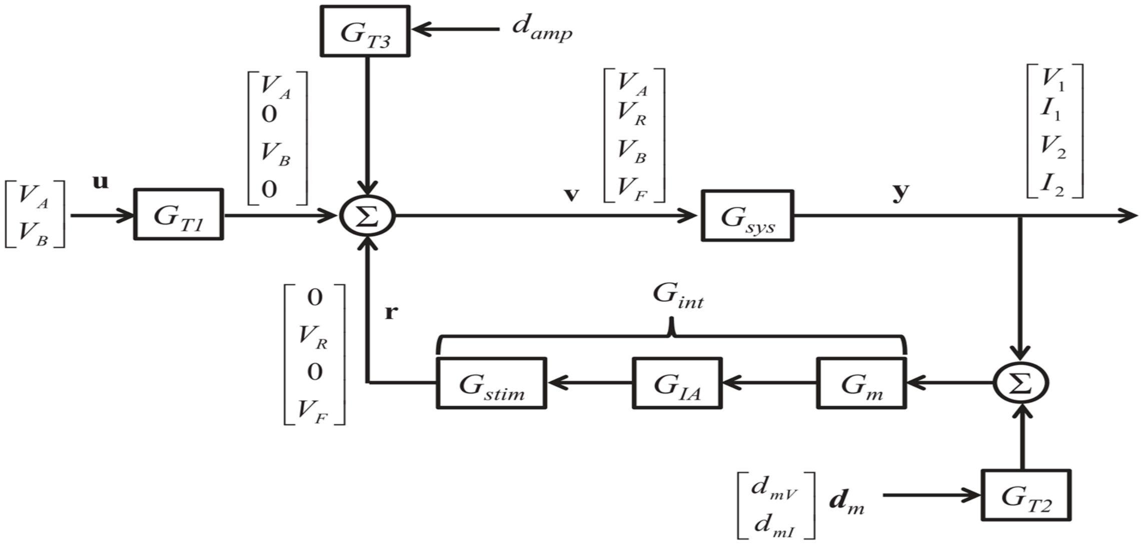
Linear Analysis Framework Using ELA for Single Phase PHIL System



Example PHIL Interface



Example PHIL Simulation Employing IA of ELA[5]

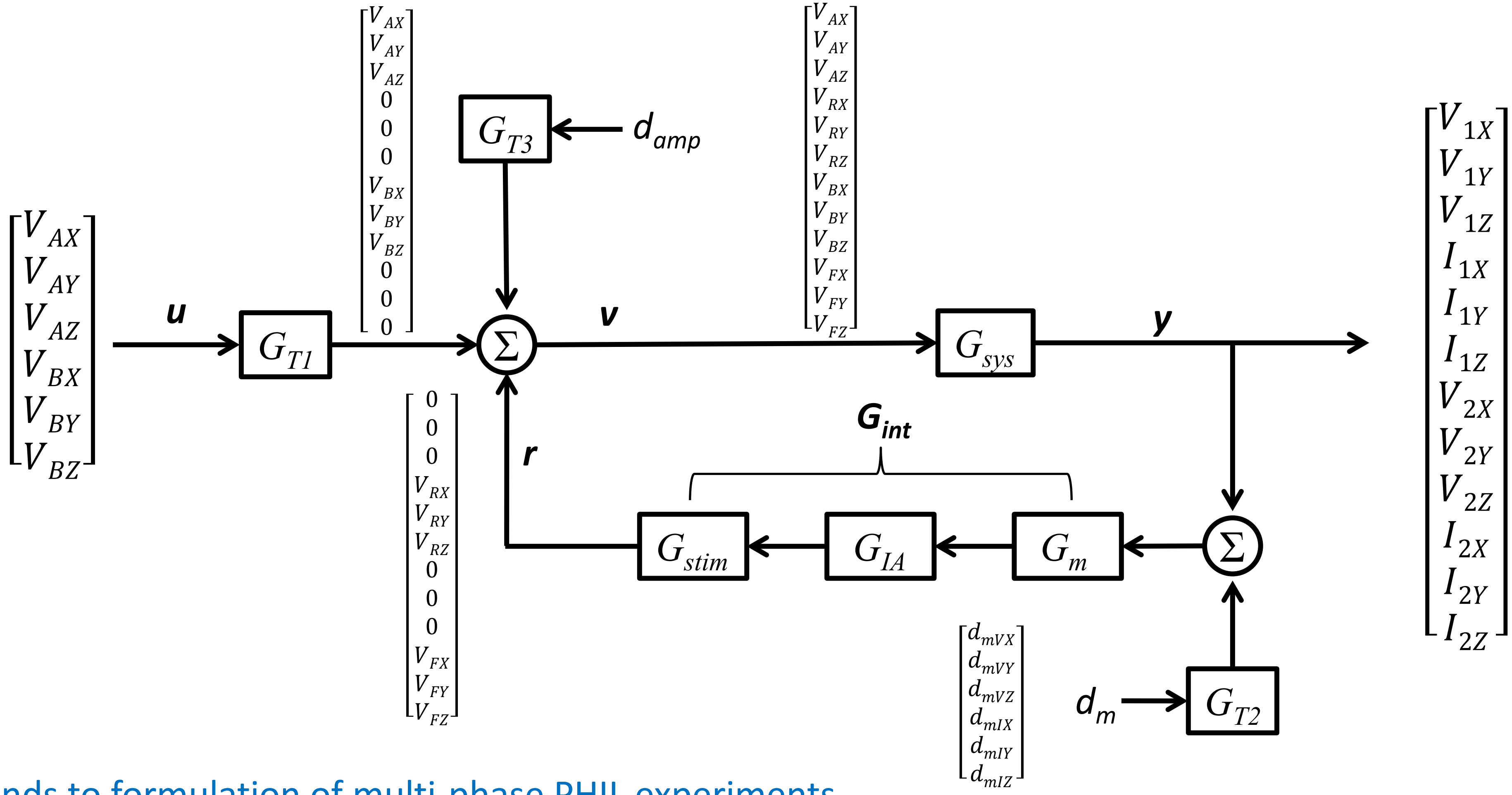


Compact formulation of PHIL experiment in terms of ELA[5]

G_{sys} – Mapping from inputs and stimuli to observable quantities
G_{int} – Represents PHIL interface
G_m – Effect of voltage and current sensors
G_{IA} – IA gains
G_{stim} – Effects of amplification and stimulation injections
d_m – Noise at sensors measurements
d_{amp} – Disturbance introduced through amplifier

[5]. James Langston, Karl Schoder, Michael Steurer, Chris Edrington, and Rodney G. Roberts, ‘Analysis of linear interface algorithms for power hardware-in-the-loop simulation’, IECON 2018

Linear Analysis for Multi-Phase PHIL experiments



ELA extends to formulation of multi-phase PHIL experiments.
Unified structure for variations in phases.

Will be presented at IECON'2024.