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Hardware In Loop Testing for IBRs using the RTDS™ Simulator

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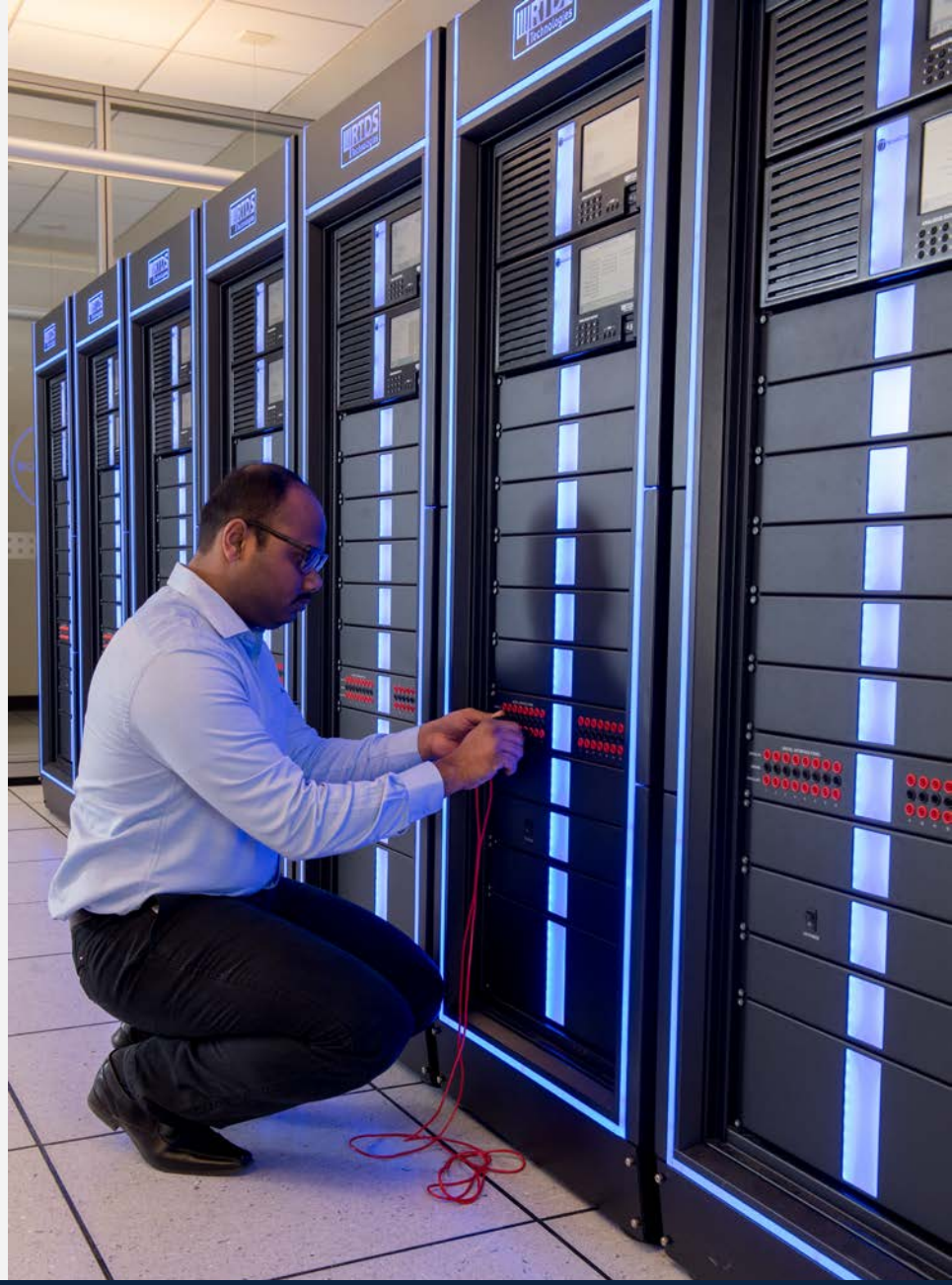
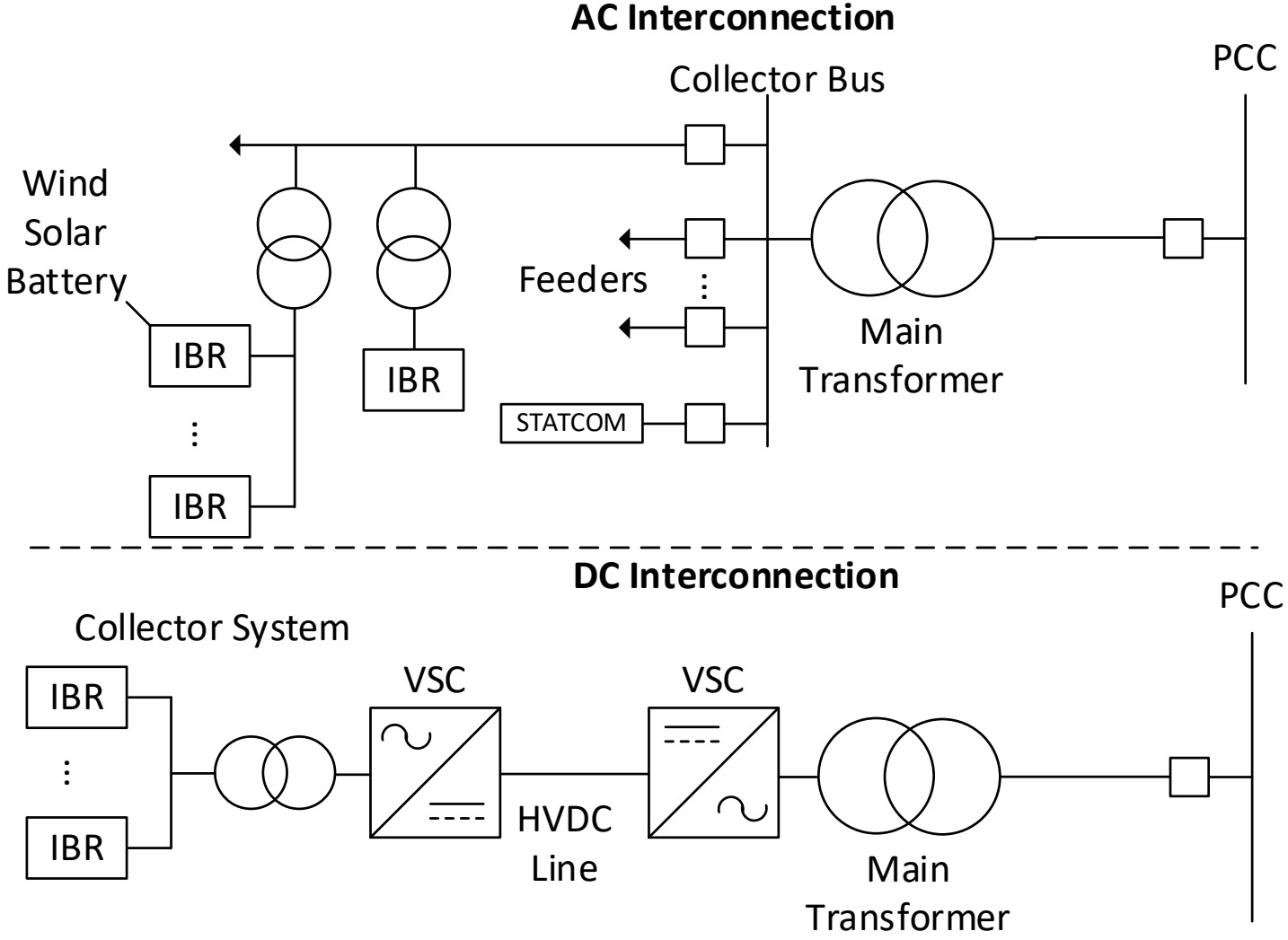
AGENDA

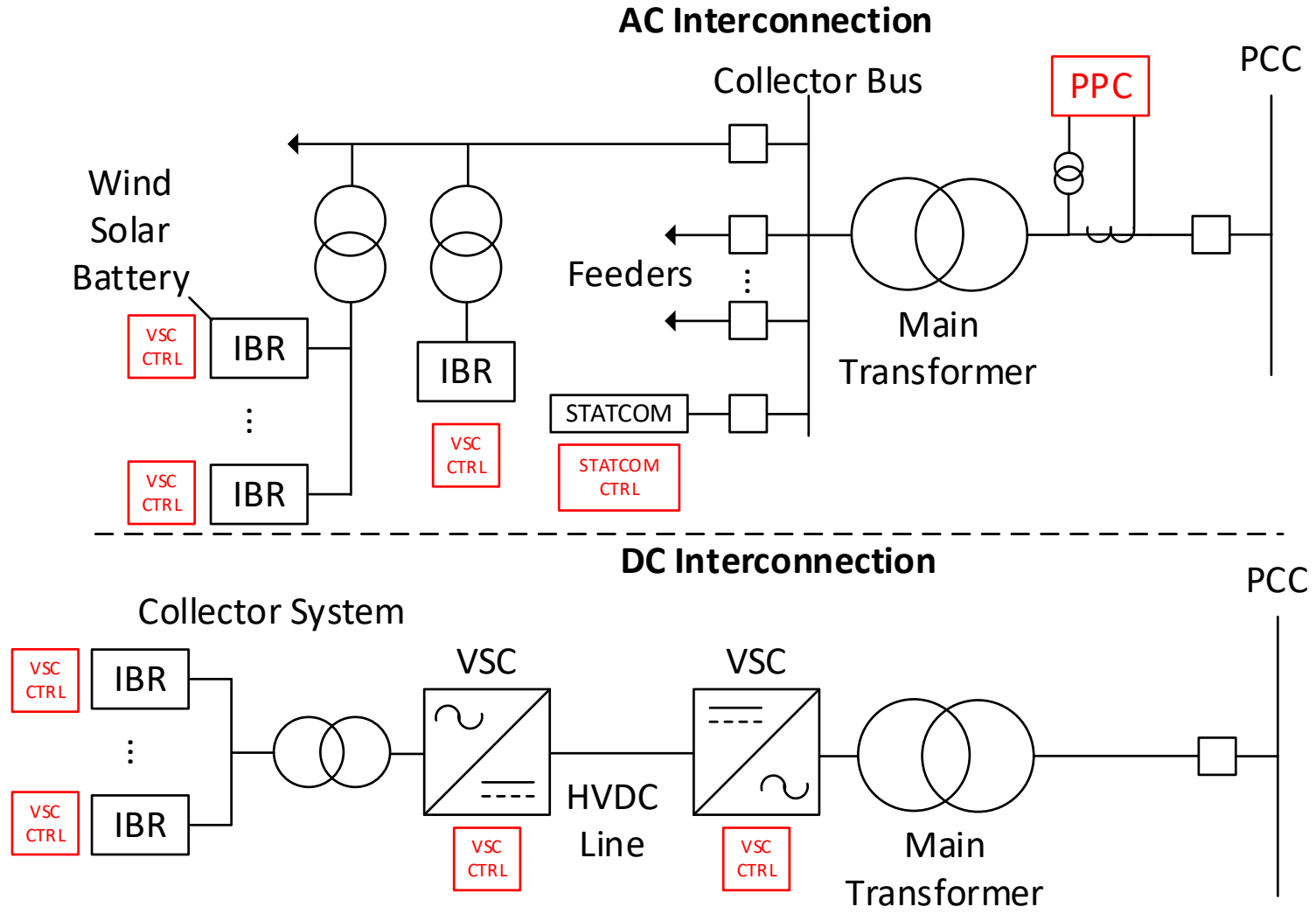
- Typical AC/DC Intercon. for IBRs
- Modeling & Simulation
- Hardware In Loop Testing
  - SIL, CHIL, PHIL
- Questions and Answers



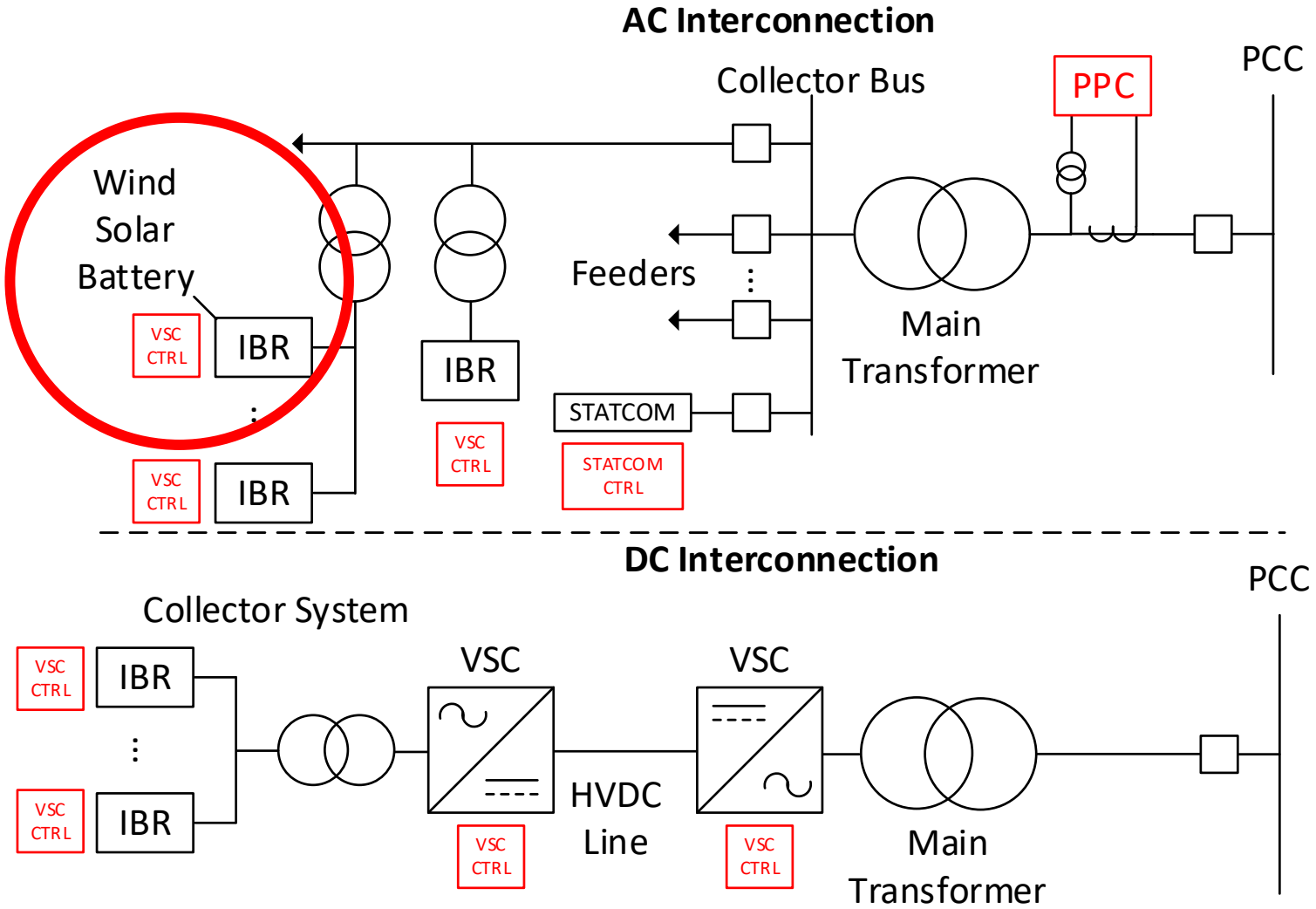
TYPICAL AC/DC IBR INTERCONNECTION



TYPICAL AC/DC IBR INTERCONNECTION

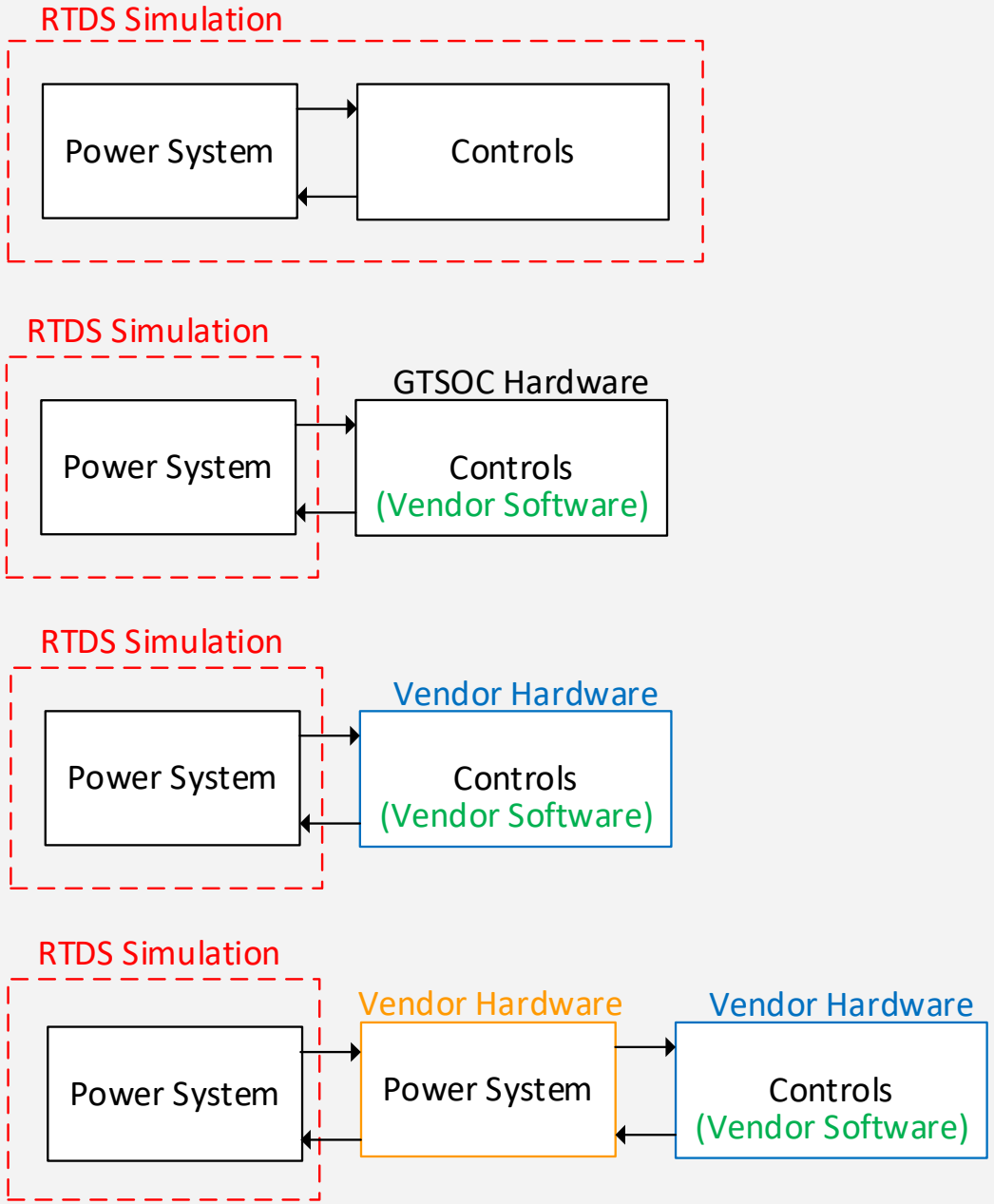


TYPICAL AC/DC IBR INTERCONNECTION



DISCUSSION POINTS

1. Modeling And Simulation
2. Software In Loop (SIL) Testing
3. Control Hardware In Loop (CHIL) Testing
4. Power Hardware In Loop (PHIL) Testing



MODELING AND SIMULATION

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2. Software In Loop (SIL) Testing
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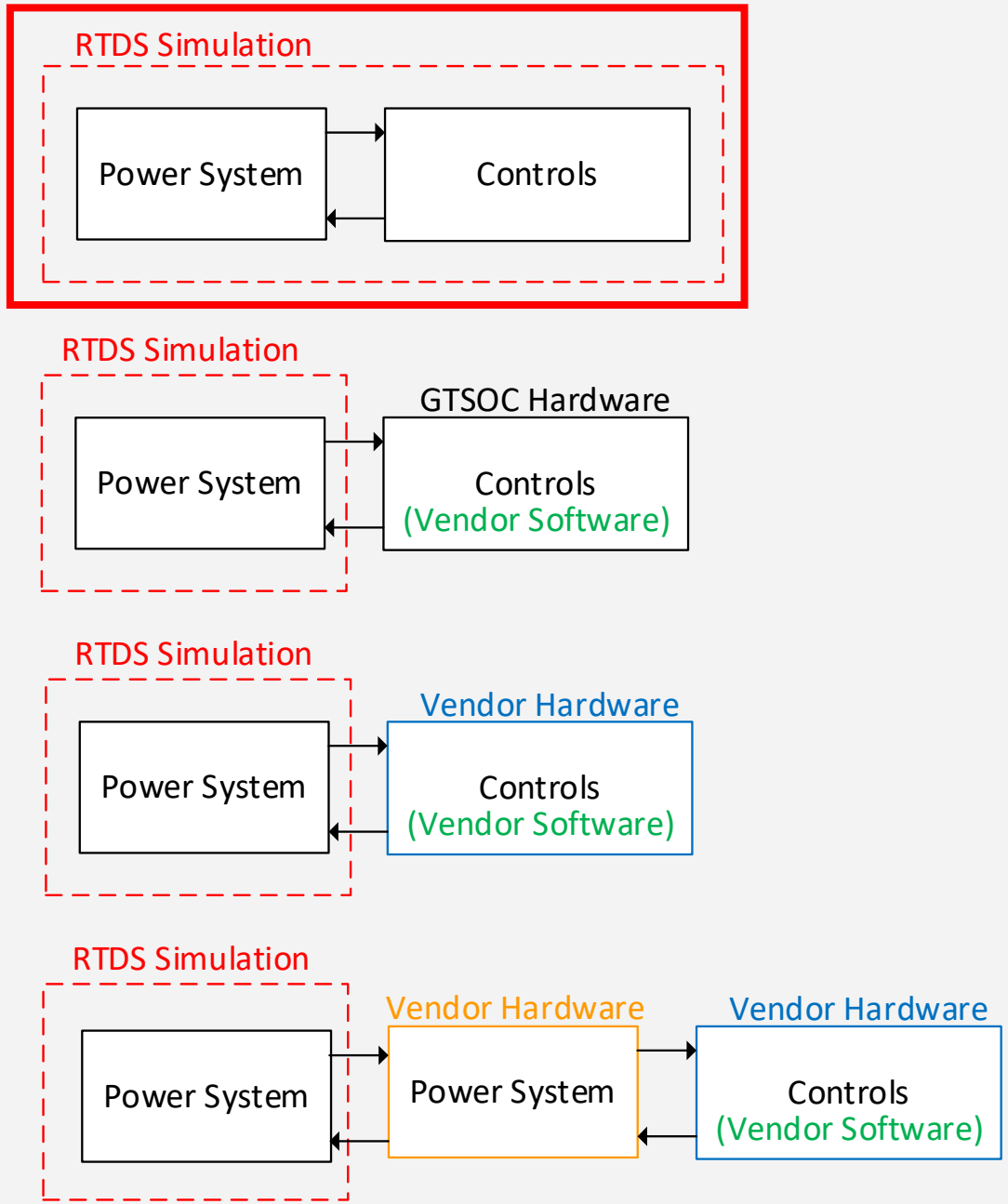
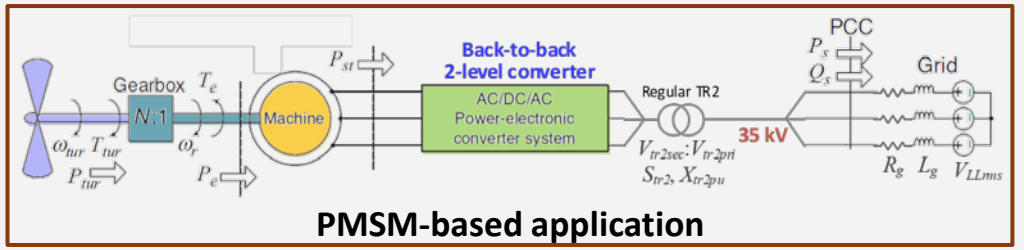
4. Power Hardware In Loop (PHIL) Testing

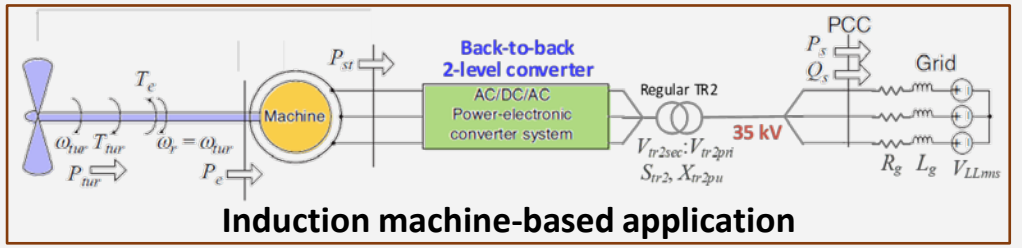


MODELING & SIM. – WIND AND SOLAR

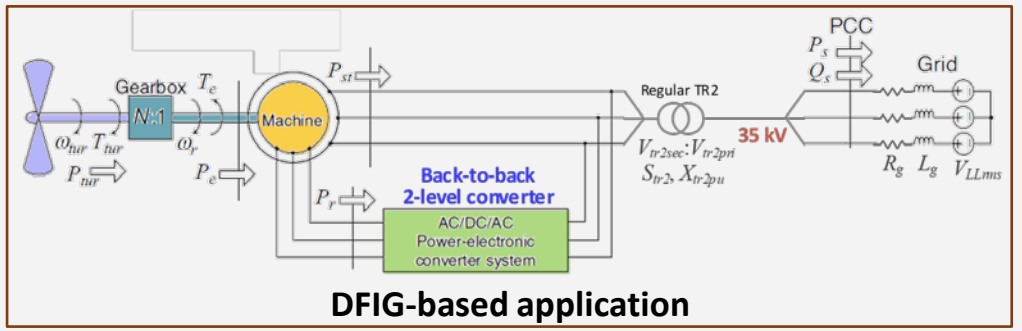
- Wind Energy Simulation
  - Type 1 – Squirrel Cage Induction Generator
  - Type 2 – Wound Rotor Induction Generator
  - Type 3 – Doubly Fed Induction Generator
  - Type 4 – Induction Machine and PMSM
- Various Machine and Turbine models available
- Power Electronic Converters modeled using Universal Converter Model (UCM)
  - AC/DC Converter models
  - DC/DC Converter Models
  - Average Value Models
  - Detailed Switching Models



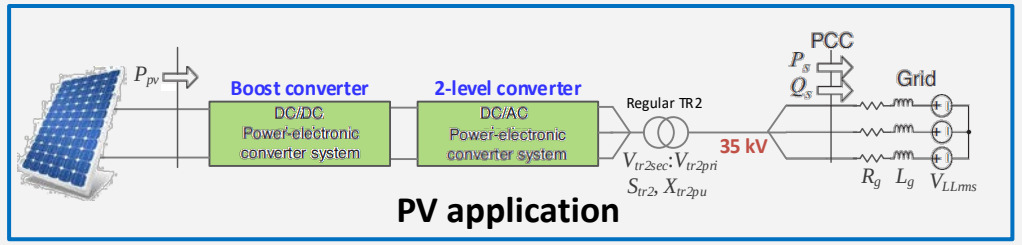
PMSM-based application



Induction machine-based application

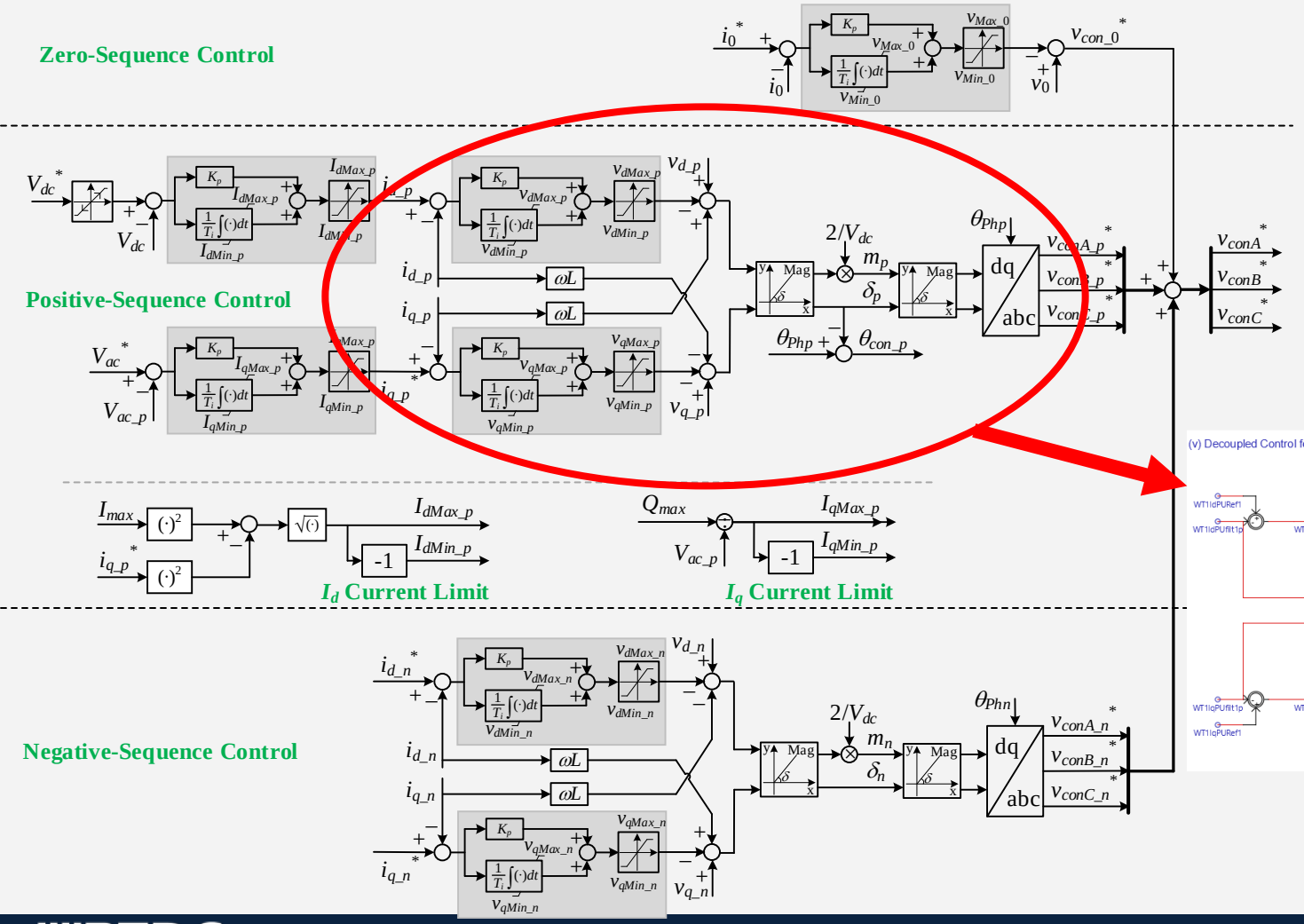


DFIG-based application

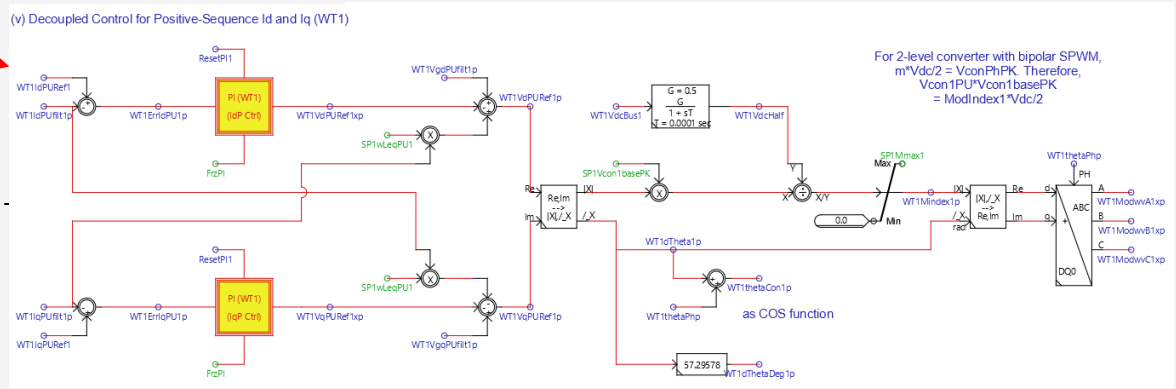


PV application

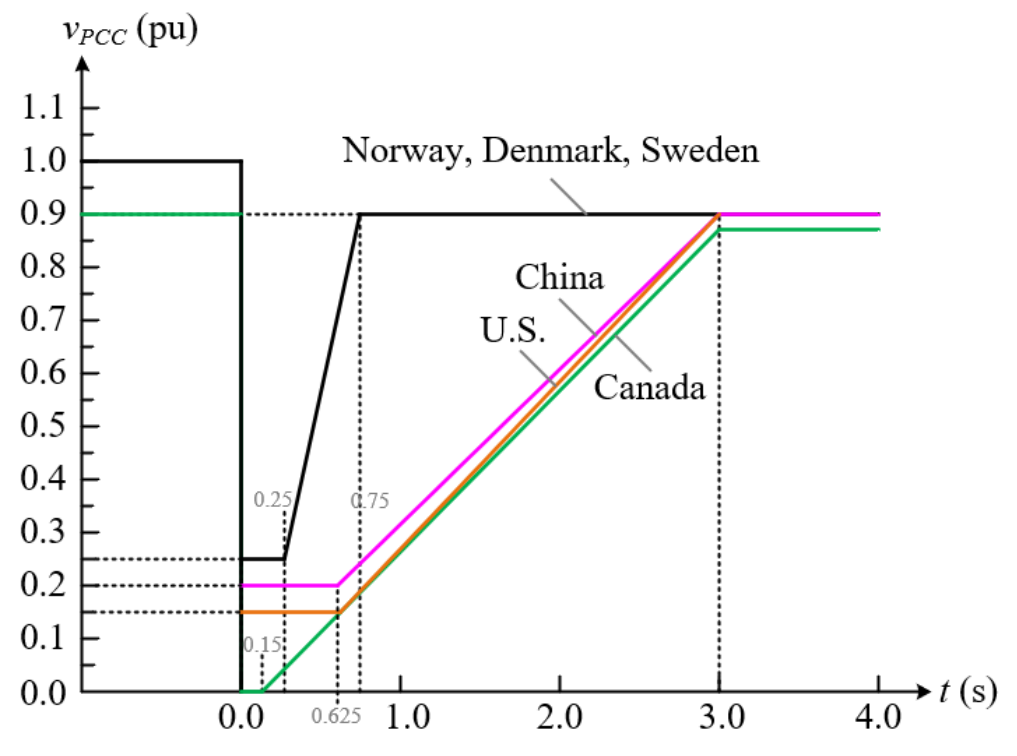
MODELING & SIM. - WINDFARM CONTROLS

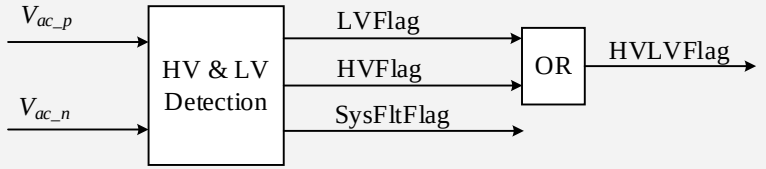


- Modeling sequence control loops
- Positive sequenve voltage/current control loops
- Negative sequence current control loops

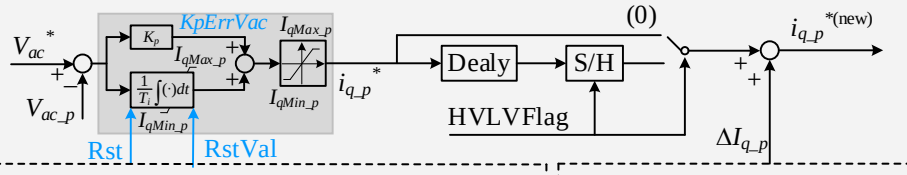


MODELING WINDFARM CONTROLS





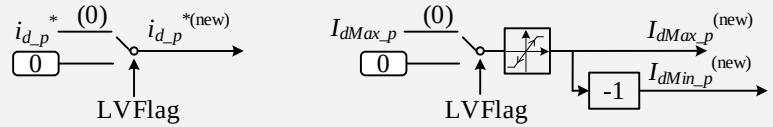
LVFlag: 0 – no LV fault; 1 – LV fault occurs.
HVFlag: 0 – no HV fault; 1 – HV fault occurs.
SysFltFalg: 0 – grid voltages are symmetrical; 1 – grid voltages are asymmetrical.



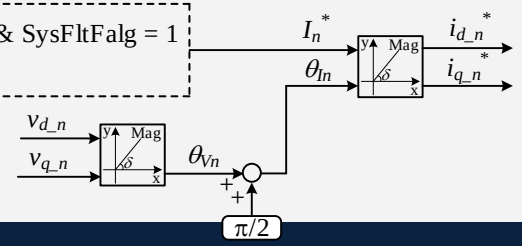
Rst = HVLVFlag

$$RstVal = \begin{cases} i_{q\_p}^{*(new)} - KpErrVac, & \text{if HVLVFlag = 1} \\ 0, & \text{otherwise} \end{cases}$$

$$\Delta I_{q\_p} = \begin{cases} K_1 \cdot (0.8 - V_{ac\_p}), & \text{if LVFlag = 1} \\ K_3 \cdot (1.1 - V_{ac\_p}), & \text{if HVFlag = 1} \\ 0, & \text{otherwise} \end{cases}$$



$$\Delta I_n^* = \begin{cases} K^- \cdot V_{ac\_n}, & \text{if LVFlag = 1 \&\& SysFltFalg = 1} \\ 0, & \text{otherwise} \end{cases}$$



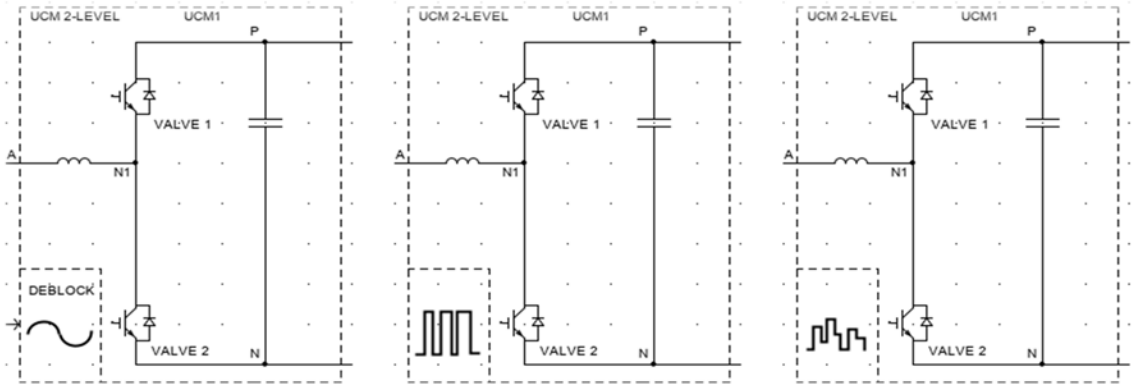
UNIVERSAL CONVERTER MODEL (UCM)

Motivation

- Demand for converter modelling and simulation with higher switching frequency (>30 kHz)
- Research found that average modelling may be used to achieve high resolution of firing
- Other average model implementation is decoupled on the DC bus – can cause instability

Solution: Universal Converter Model

- 2-level, NPC (ANPC), T-type, boost and buck, flying capacitor, DAB topologies available
- Multiple input (control) types
- Can be used in Mainstep OR Substep
- Improving performance and reducing computational burden
- **No decoupling / interface lines**



2-level UCM

SOFTWARE IN LOOP TESTING

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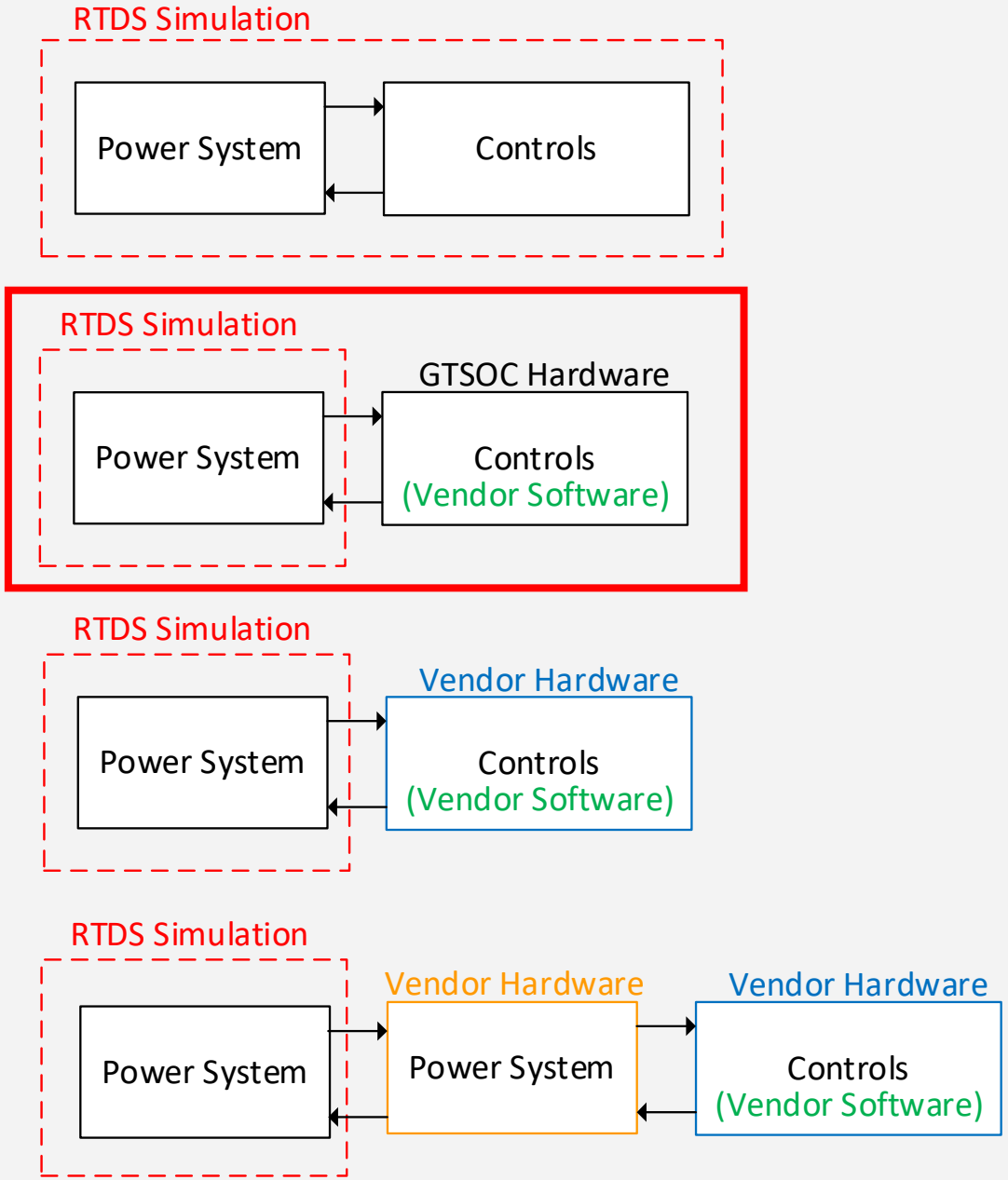
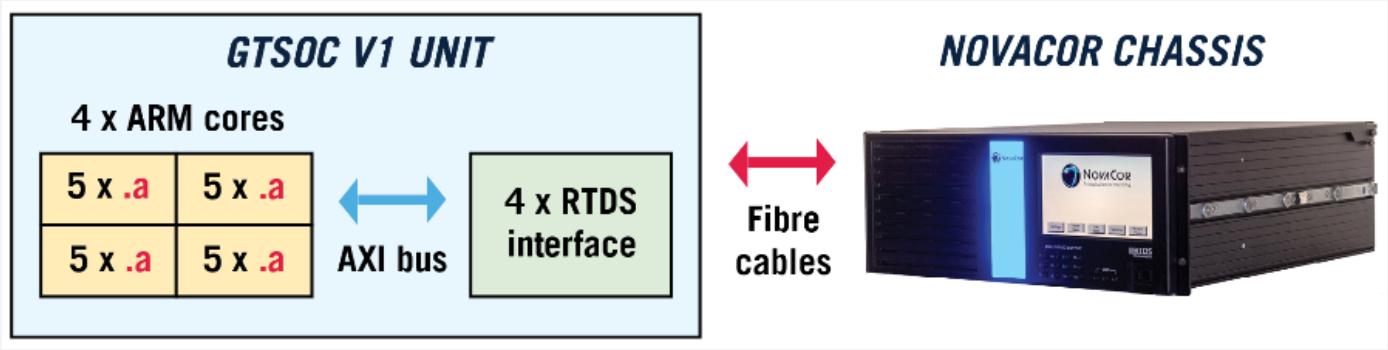


SOFTWARE IN LOOP TESTING

GTSOC Hardware

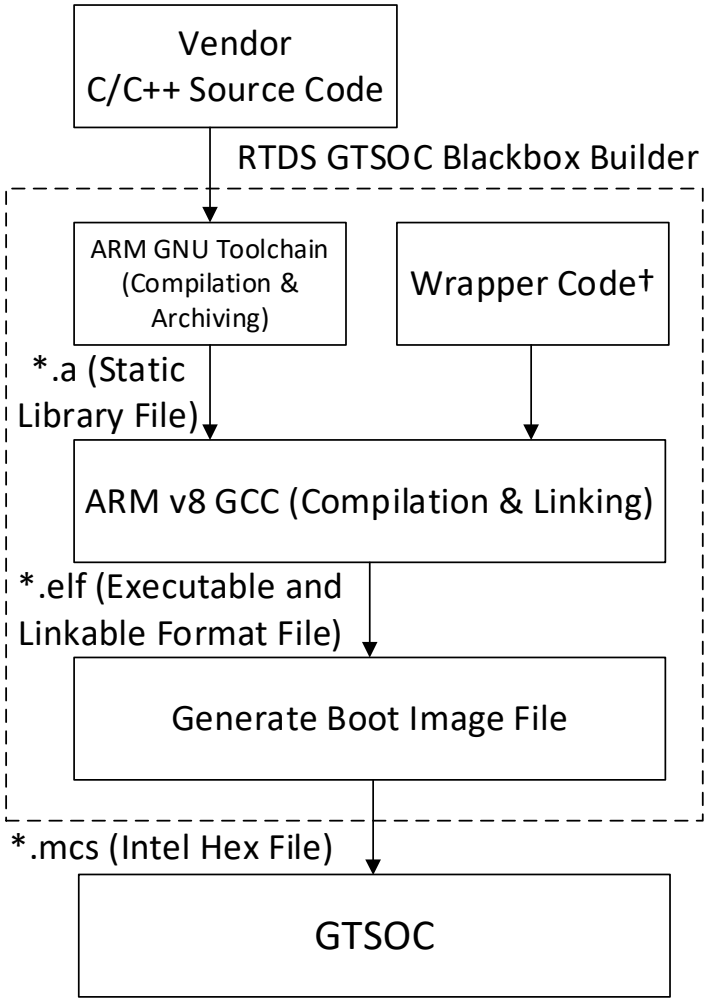
- New hardware to support execution of black box controls
- GTSOC – System-on-Chip
- Combination of FPGA and Multi-Processor System-on-Chip (MPSoC)
- Supports Bare Metal Execution of Static Library (*.a) Files containing Vendor Source Code
- Interconnects with NovaCor via Fiber Optic Cables



SOFTWARE IN LOOP TESTING

Deploying Blackbox Controls on the GTSOC

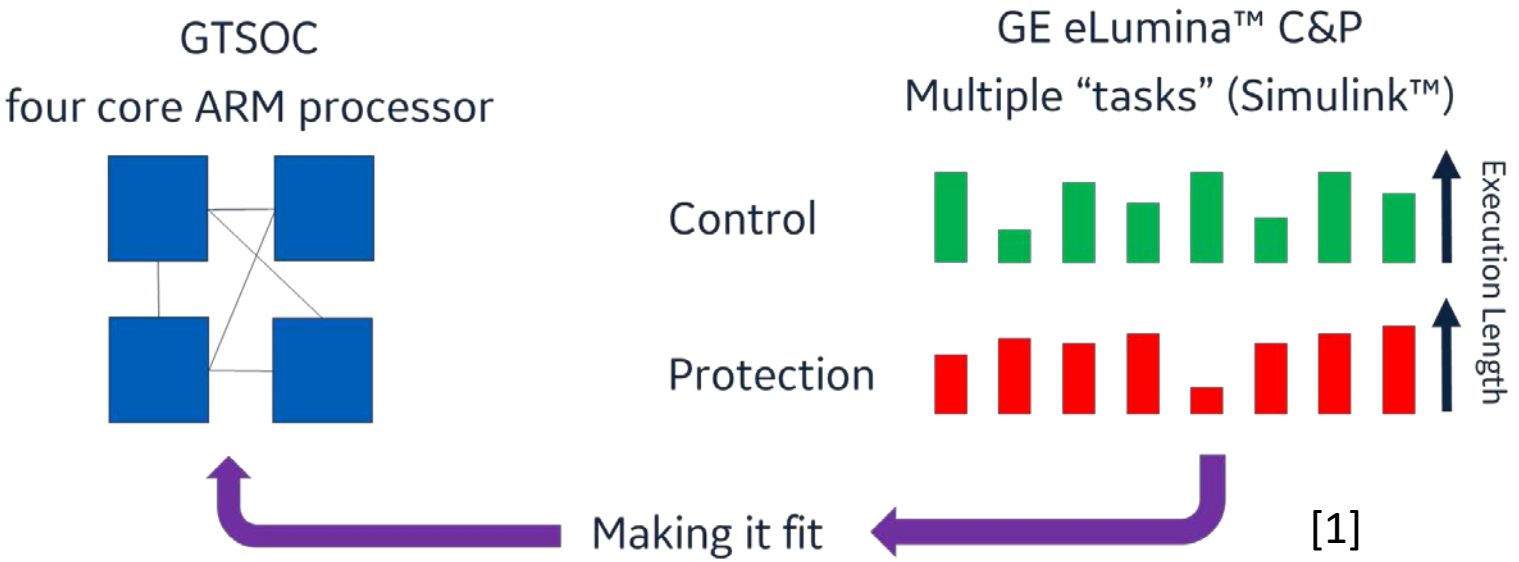
- Vendor C/C++ Source Code
  - Written by Hand
  - Generated via MATLAB/Simulink
- RTDS GTSOC Blackbox Builder Tool
  - Source code compiled into Static Library (*.a)
  - Wrapper code is used for mapping inputs/outputs and parameters
  - Generates Firmware (*.mcs) for GTSOC
- Templates are Provided for Wrapper Code



SOFTWARE IN LOOP TESTING

GE Vernova HVDC control and protection on GTSOC

- Runs complete control and protection code from the original source model
- Multiple challenges overcome
  - Determining the number of GTSOC ARM cores required to model the control and protection system and assure real time performance
  - Evaluating the latency in the simulation setup



[1]

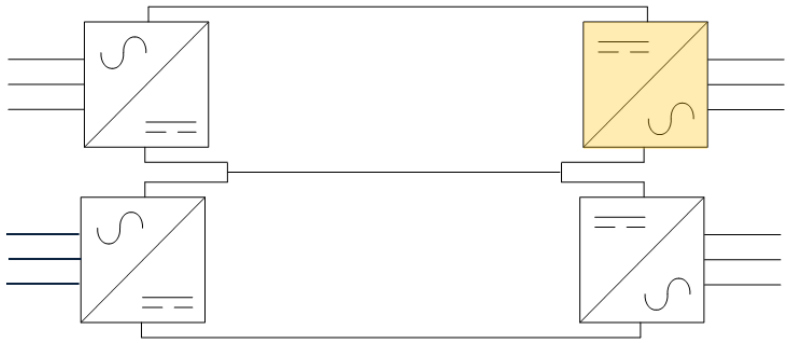
SOFTWARE IN LOOP TESTING

GE Vernova HVDC control and protection on GTSOC

- Four ARM cores required for Control
- Four ARM cores required for Protection

Symmetrical Monopole

Bipole



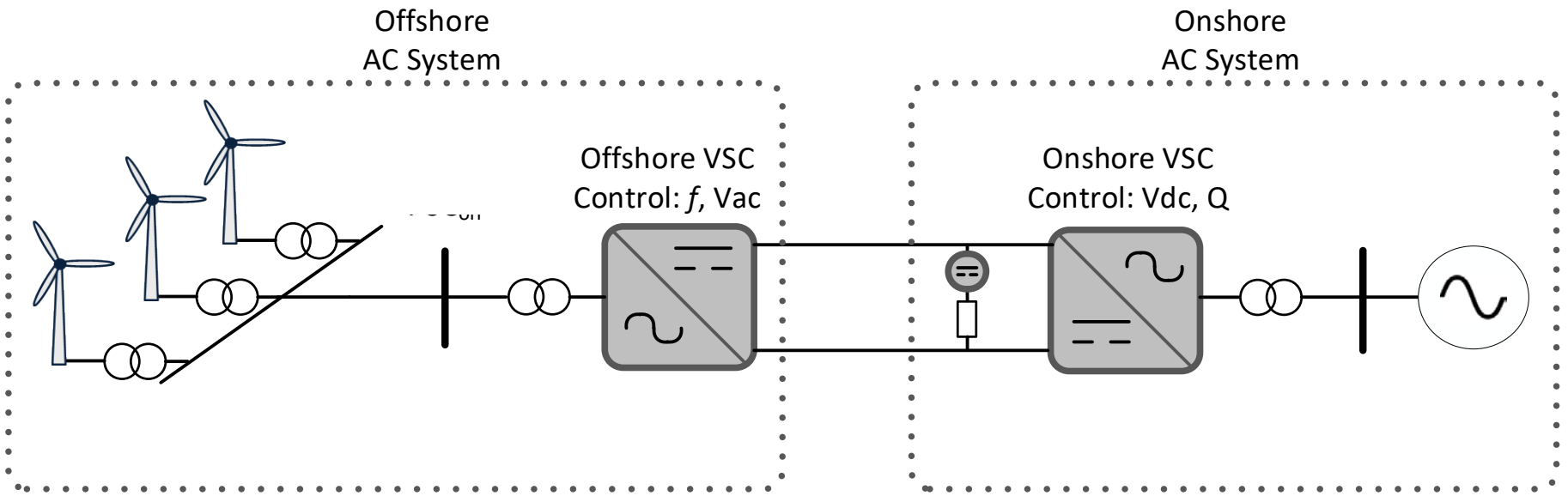
One pole-end

[1]

SOFTWARE IN LOOP TESTING

GE Vernova HVDC control and protection on GTSOC

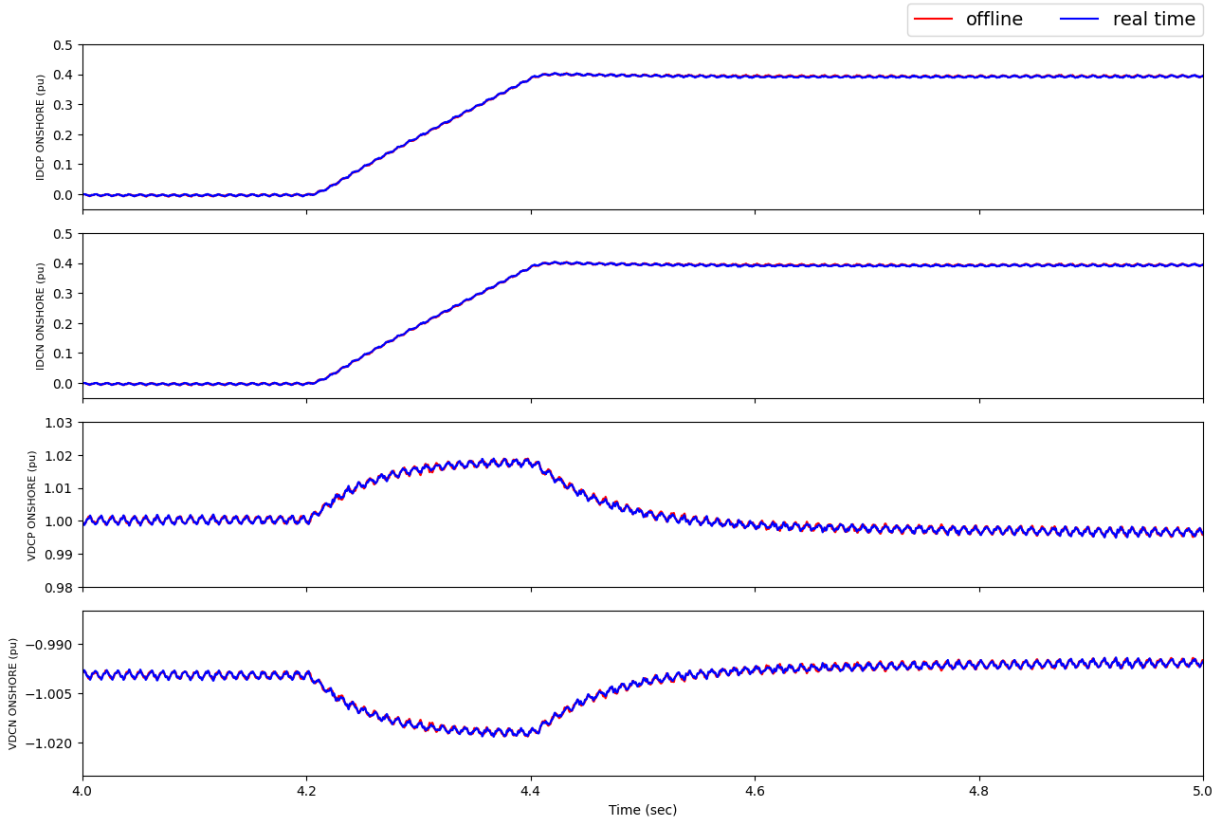
- Used for benchmarking against offline model
- Onshore and Offshore converters' control and protection modelled on GTSOC
- 4 GTSOC units - 16 ARM cores
- 1 NovaCor Chassis – 2 cores
- Compared results to offline model, did not optimize C&P



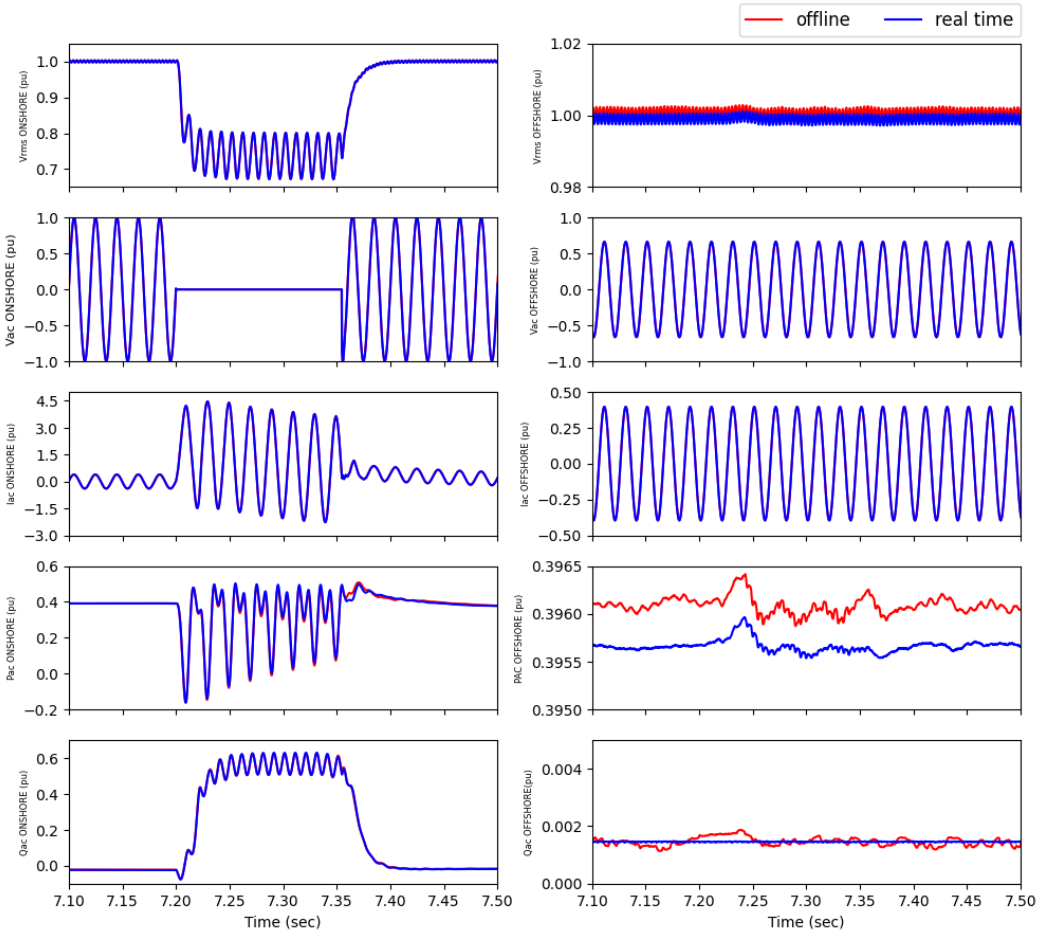
[2]

SOFTWARE IN LOOP TESTING

GE Vernova HVDC control and protection on GTSOC



Power Ramp (DC signals)



150 ms 1-phase fault at Onshore POC

CONTROL HARDWARE IN LOOP TESTING

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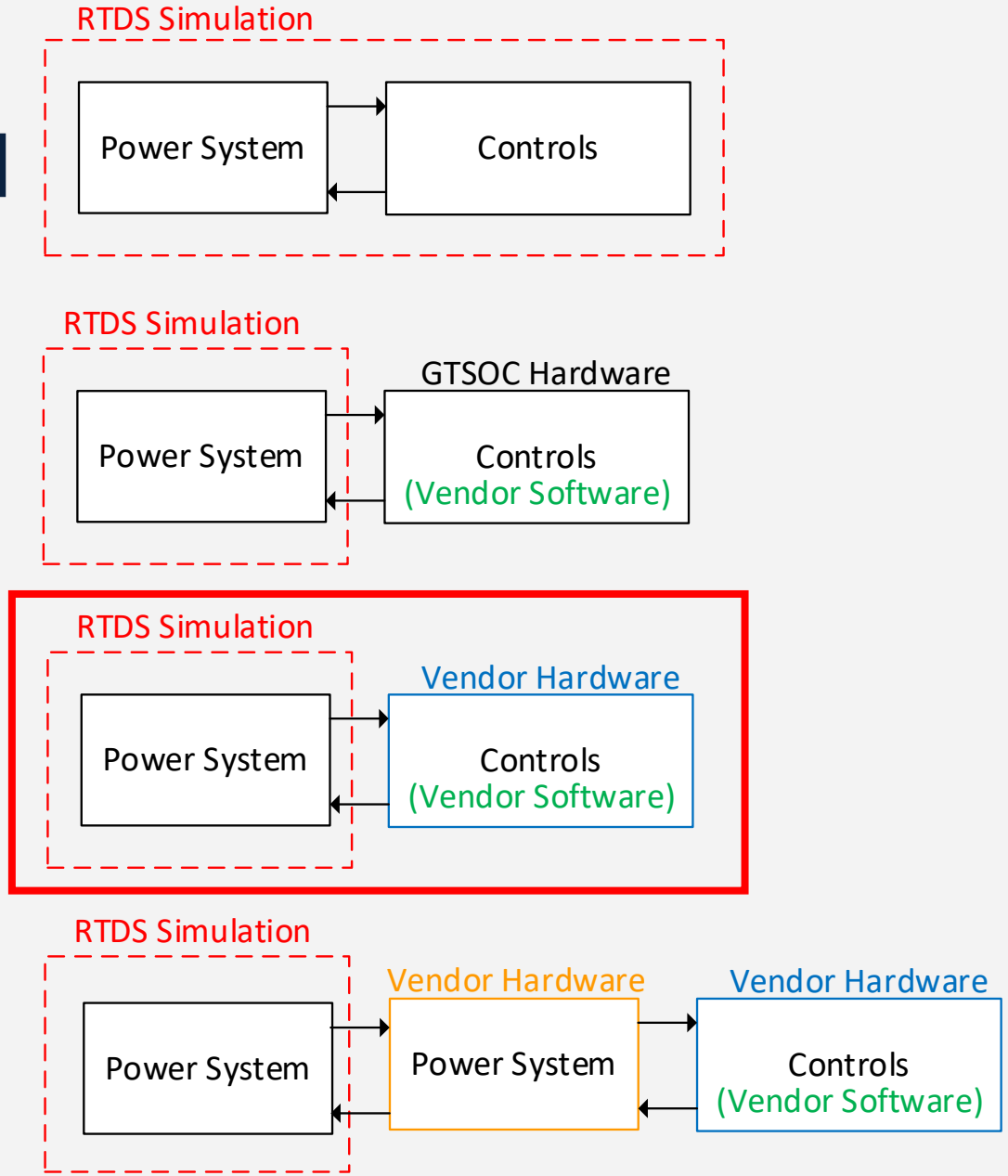
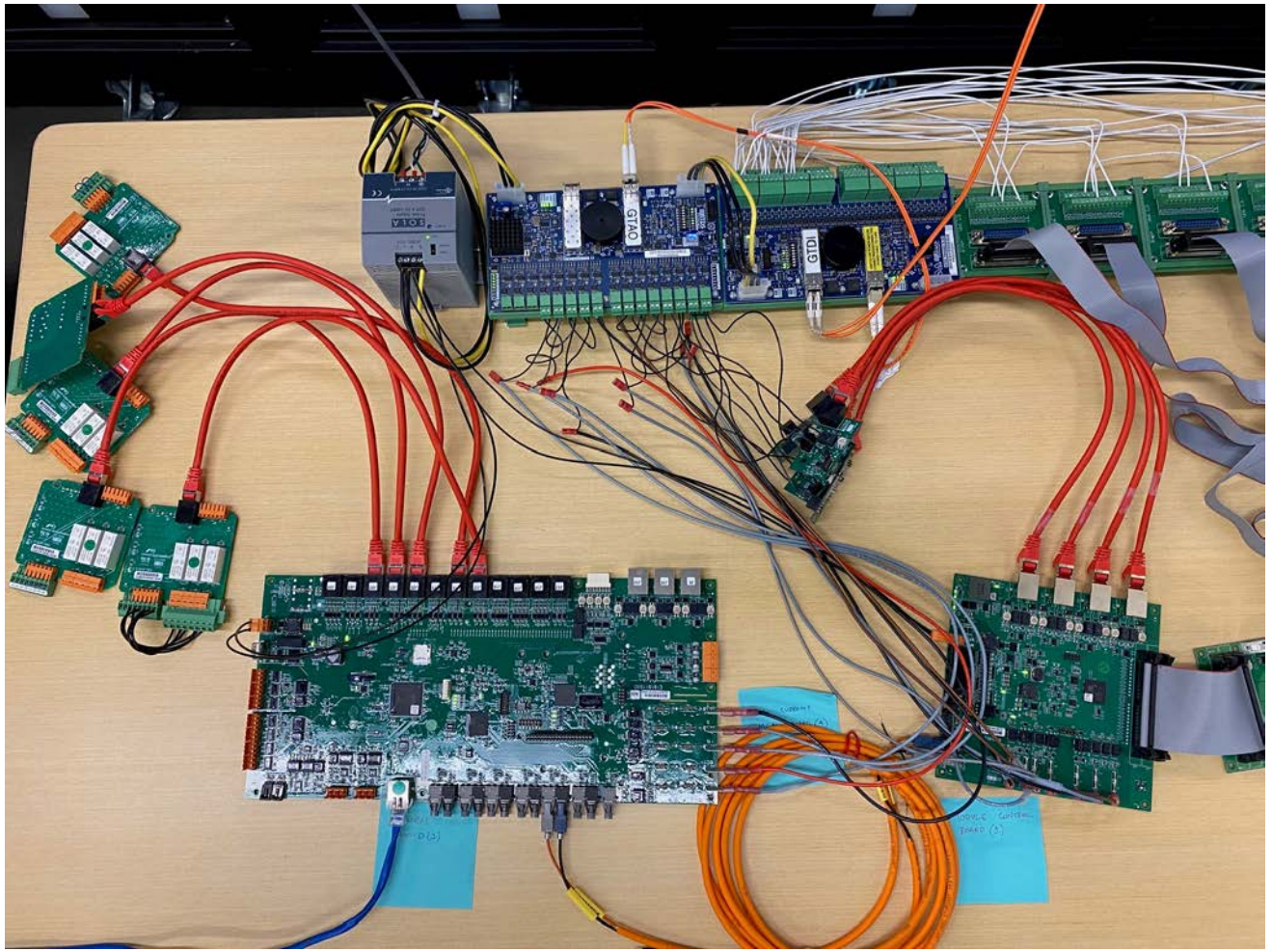


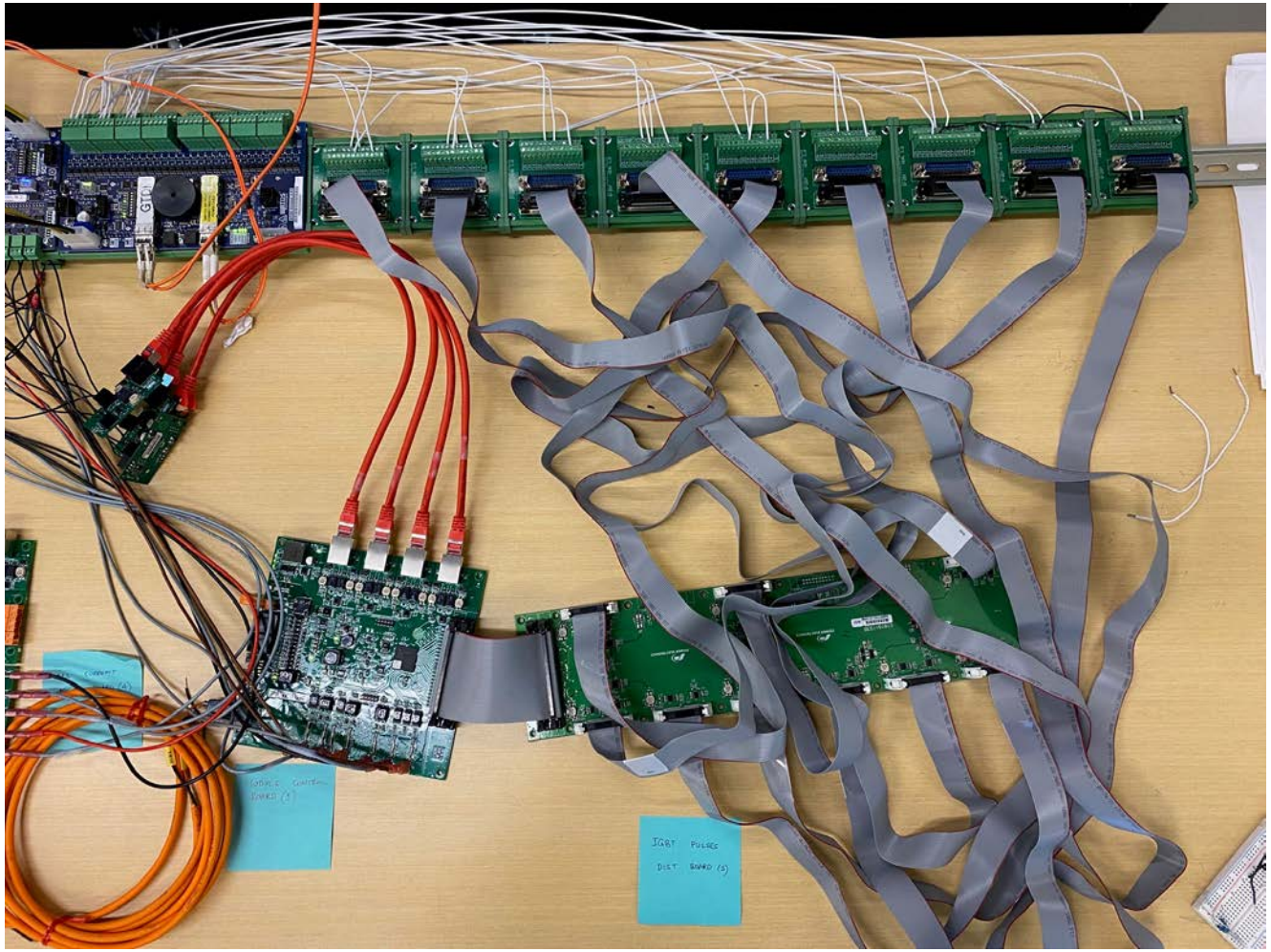
CONTROL HARDWARE IN LOOP TESTING

- Central control board
- Current measurement board
- Current measurements provided via GTAO



CONTROL HARDWARE IN LOOP TESTING

- Pulse distributor board
- Firing pulses input via GTDI
- UCM model supports GTDI input with Improved Firing



POWER HARDWARE IN LOOP TESTING

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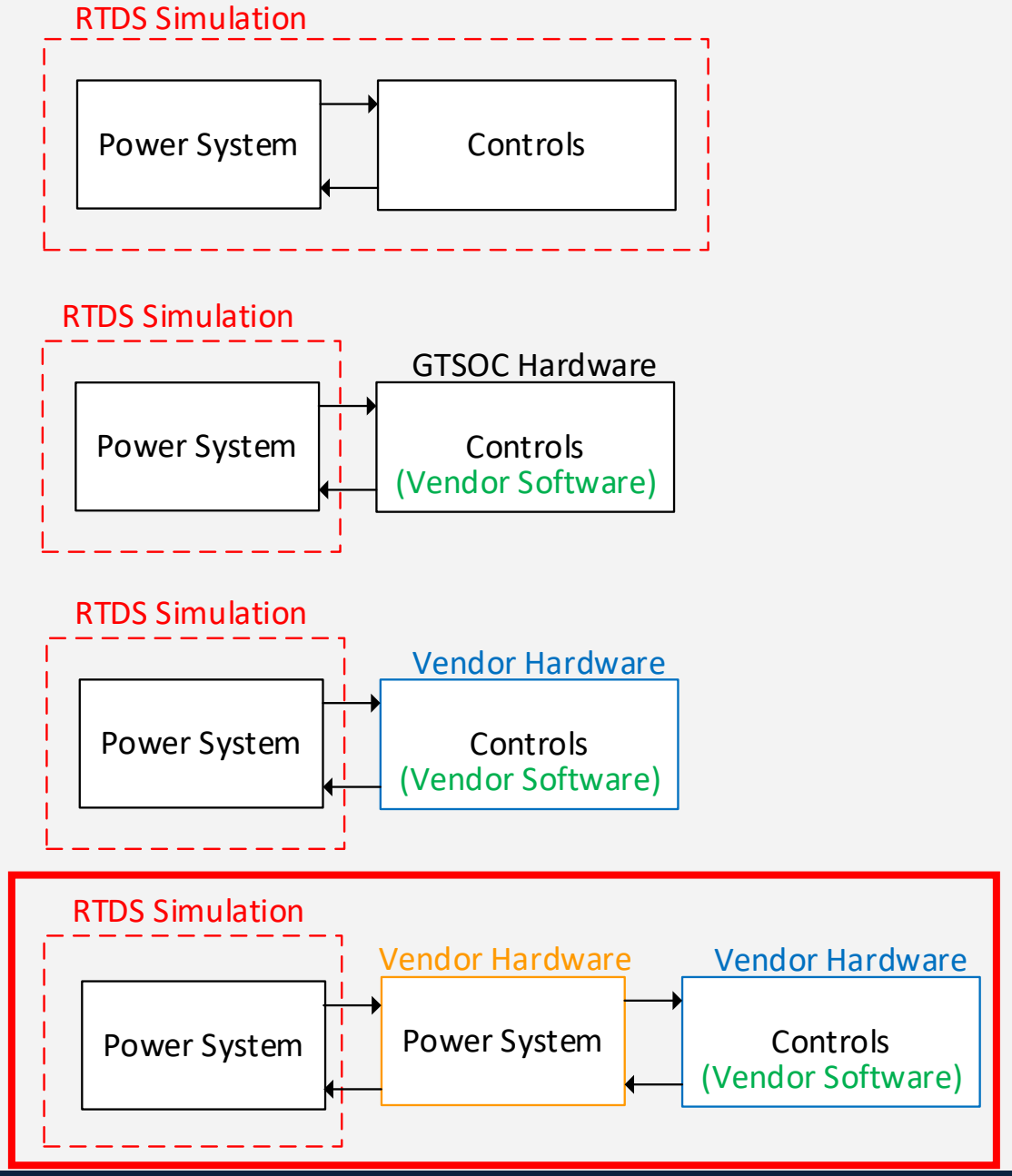
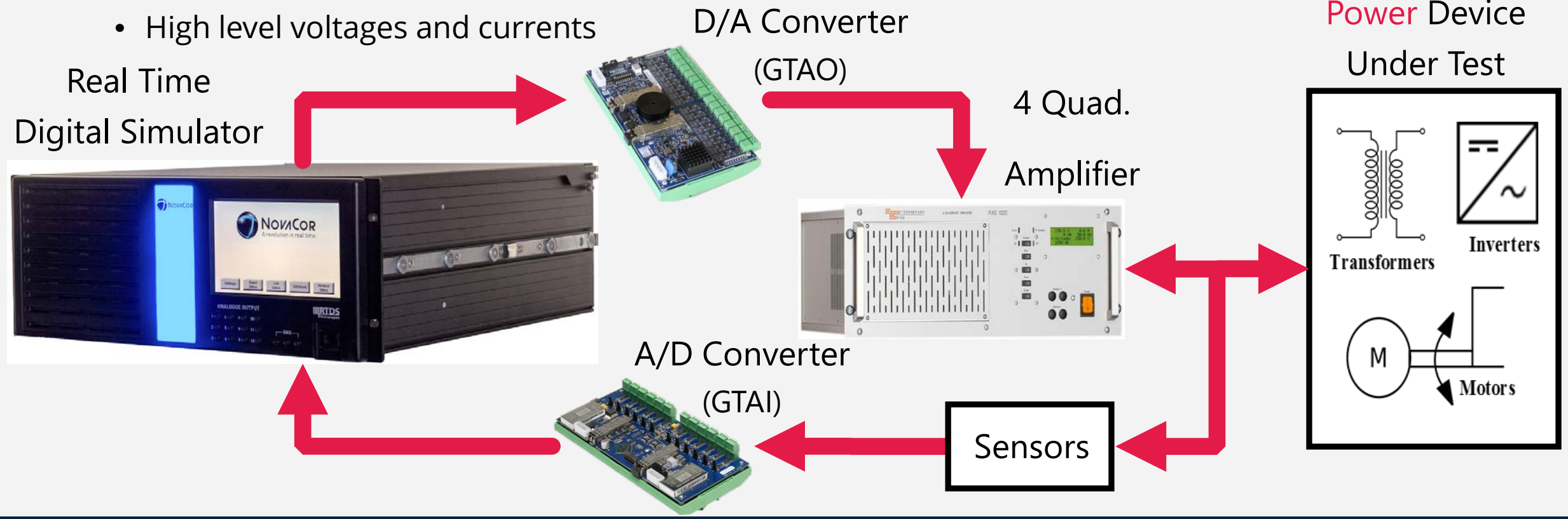


POWER HARDWARE IN LOOP TESTING

- A portion of the power system is modeled in RTDS
- Power exchange via 4 quadrant amplifier
- High level voltages and currents

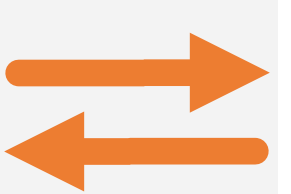


POWER HARDWARE IN LOOP TESTING

- Aurora Communication Protocol
- Reduced loop delay & noise
- Improved stability & accuracy

RTDS

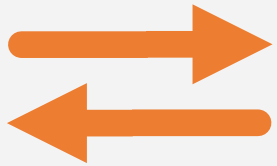
Aurora Interface



SPS APS Amplifier

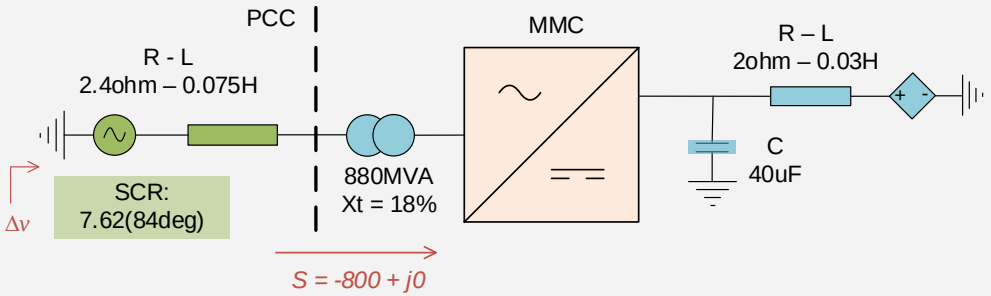
RTDS

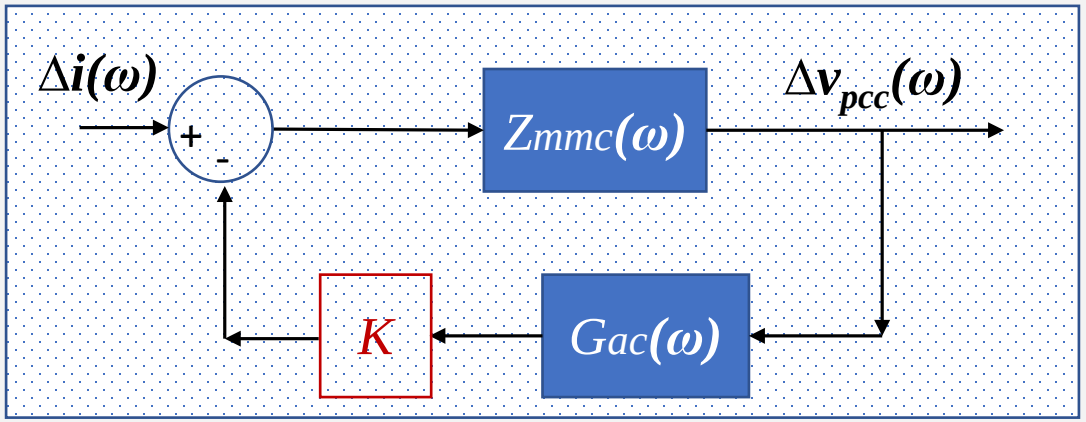
Aurora Interface

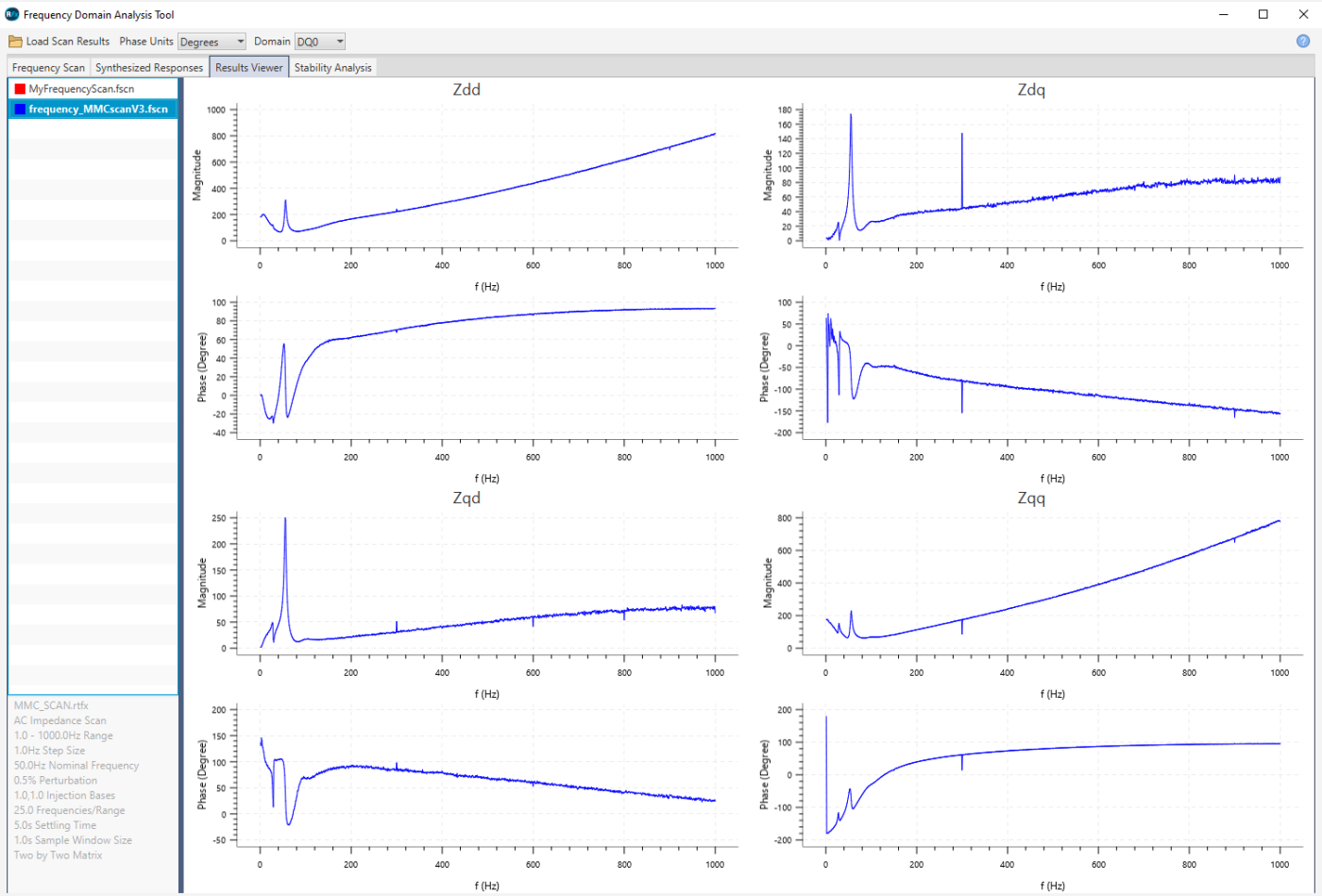


EGSTON COMPISO System

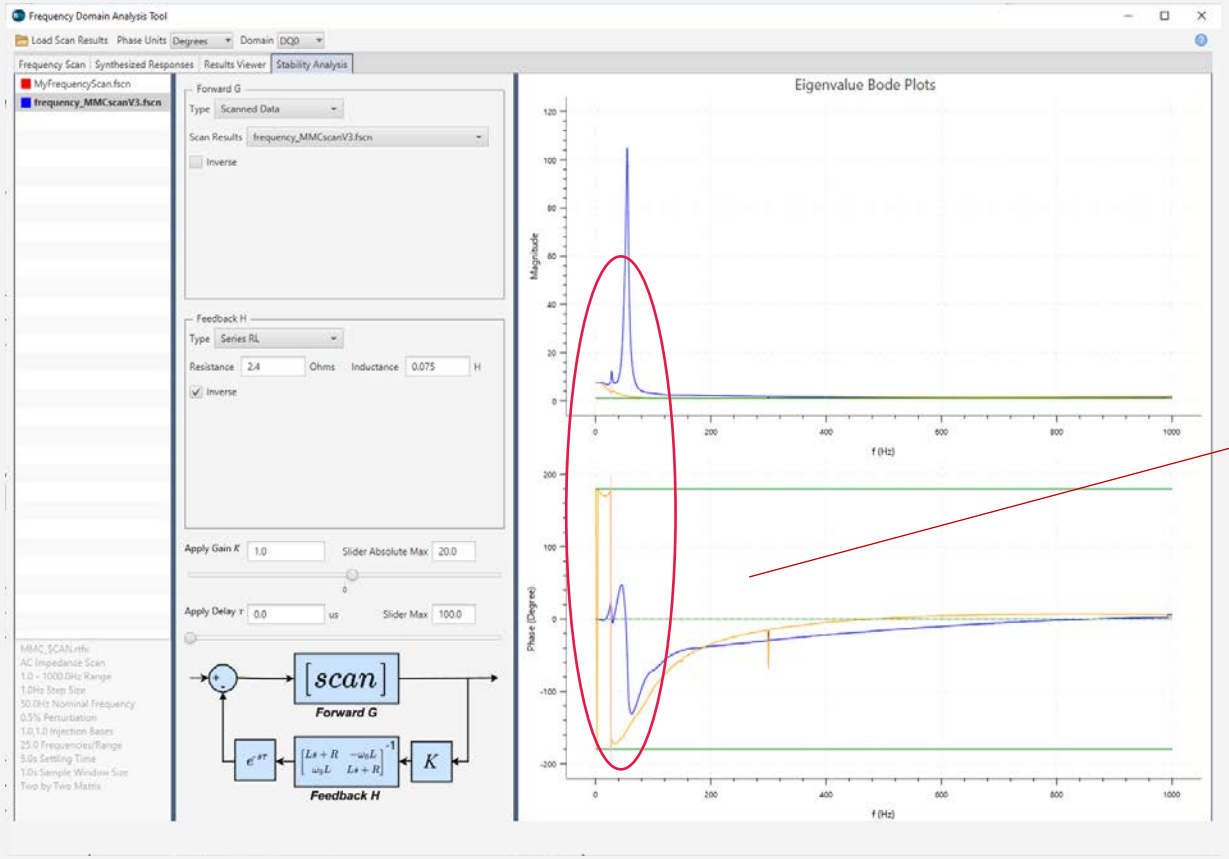
FREQUENCY SCAN

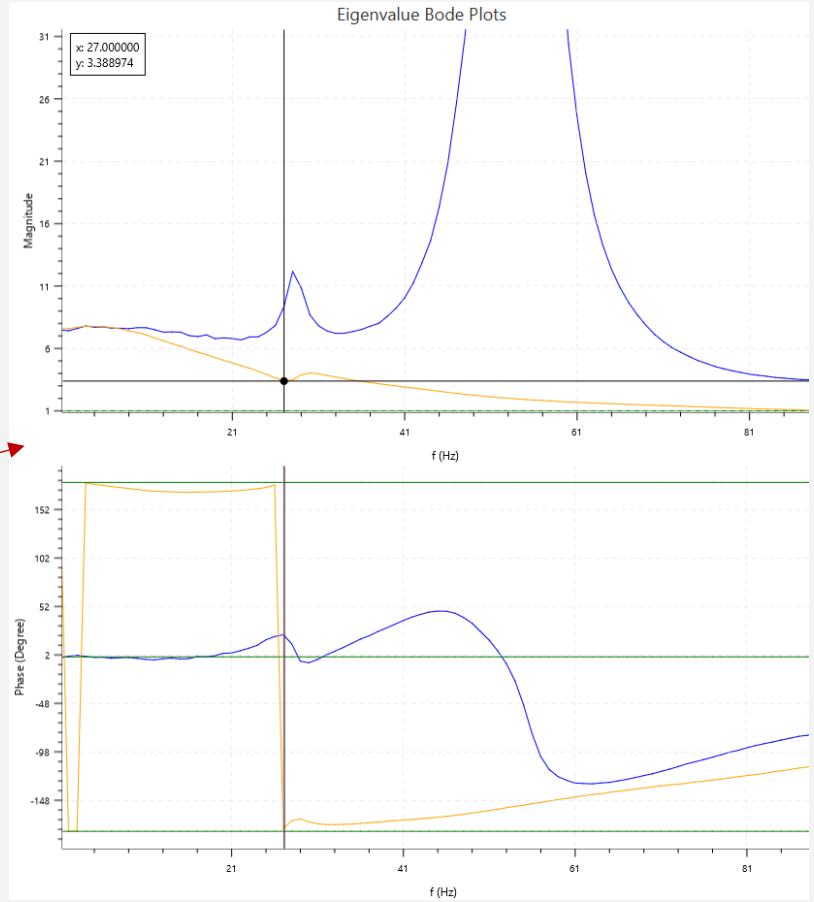






FREQUENCY SCAN





Phase Angle Crossing ± 180 for the MMC Scan Case

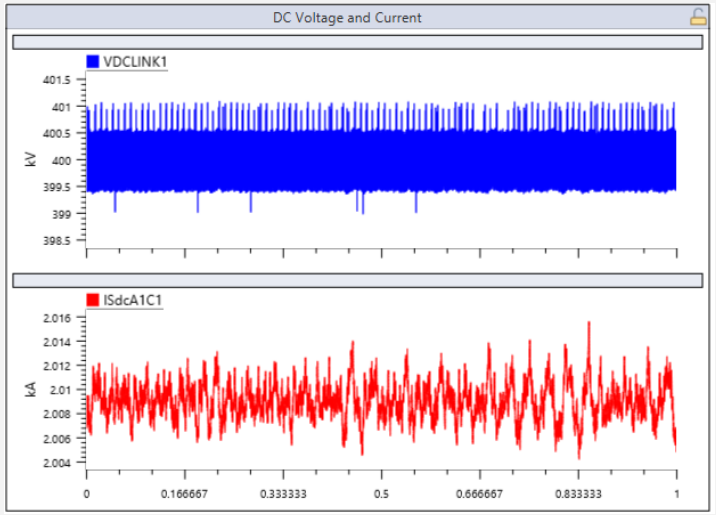
"Stability Analysis" Tab in FDA for the MMC Scan Case (SCR=7.62)

Two frequencies where angle crosses +/- 180 degrees

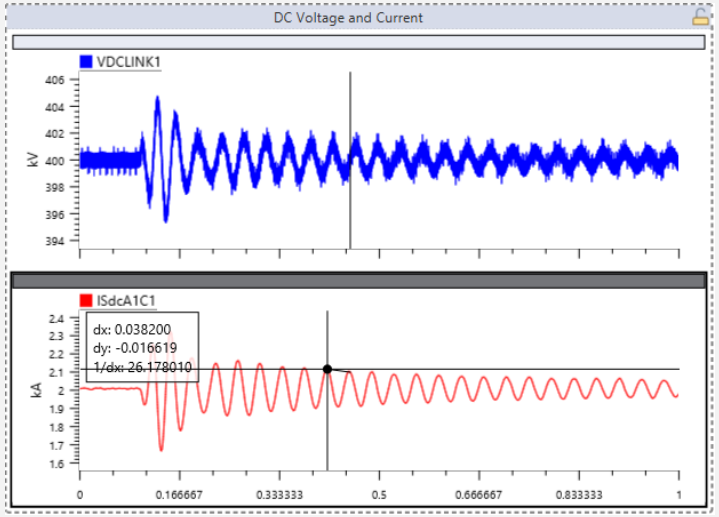
~3hz → magnitude is 7.70; ~26-27 Hz → magnitude is ~3.46 (Critical Freq.)

$$CSCR = \frac{SCR}{GM} \rightarrow \text{CSCR ~= 2.2}$$

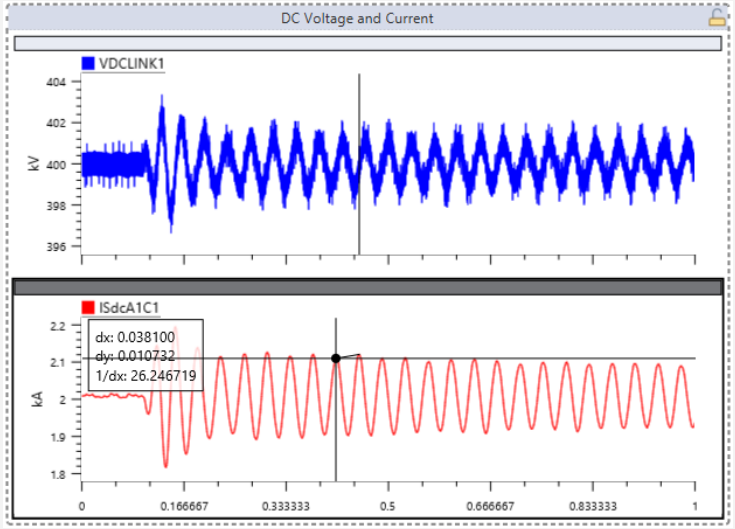
FREQUENCY SCAN



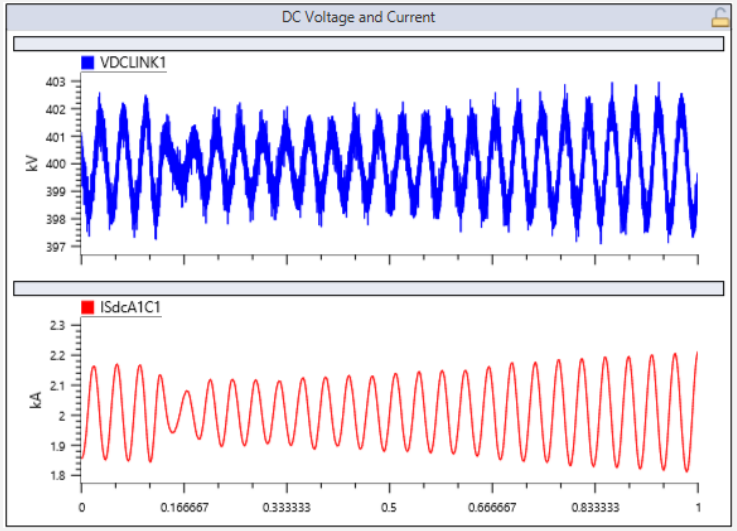
SCR: 7.62



SCR: 2.5 -> 2.3



SCR: 2.3 -> 2.2



SCR: 2.2 -> 2.15

- From simulation, it is observed that marginal stability point is around **SCR 2.2** and the oscillation frequency is around **26-27 Hz**
- Matches to frequency scan result of marginal stability

Oscillation magnitude rises and eventually blows up!

THANK YOU!
QUESTIONS?

[1] Implementation of GE Vernova MMC Controls on GTSOC platform, RTDS Technologies, Aug 2023
[2] C. Barker et al. “Software in the Loop Real Time Simulation of a HVDC Terminal”, CIGRE Paris 2024

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