



NOVICOR™

A revolution in real time.

PHIL Developments to Improve
Stability Margins

WRTDS
Technologies





Presentation Outline

Review of PHIL

Open Loop vs Closed Loop

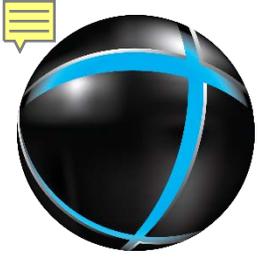
Key Factors for PHIL Simulation

Recent Developments

Recent PHIL Work (Aurora Interface)

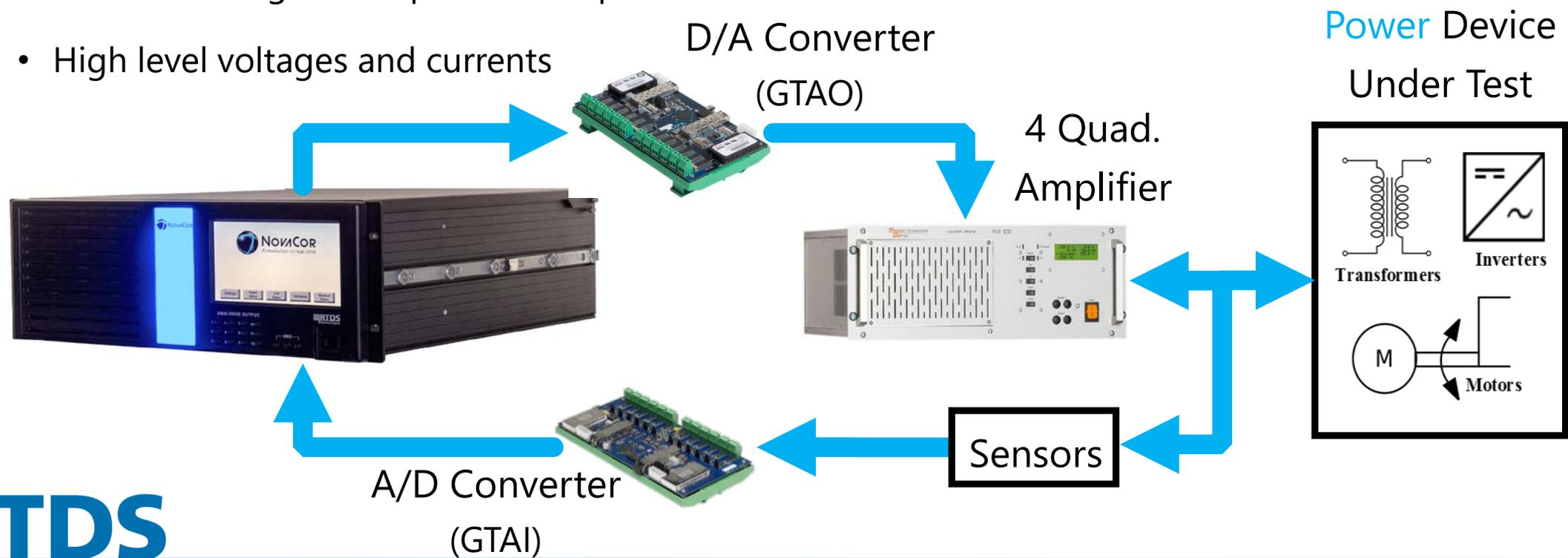
Future PHIL Work





Power Hardware In Loop (PHIL)

- In PHIL,
 - A portion of the power system is modeled in RTDS
 - Power exchange via 4 quadrant amplifier
 - High level voltages and currents

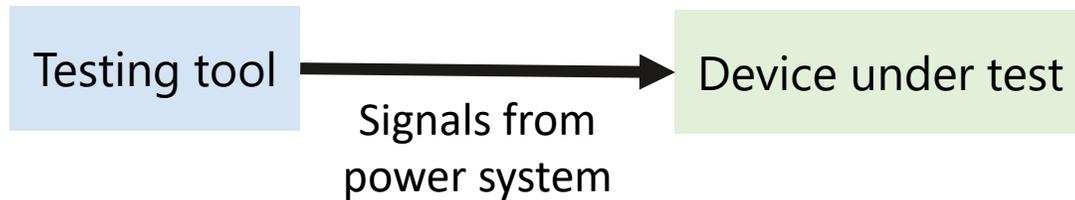




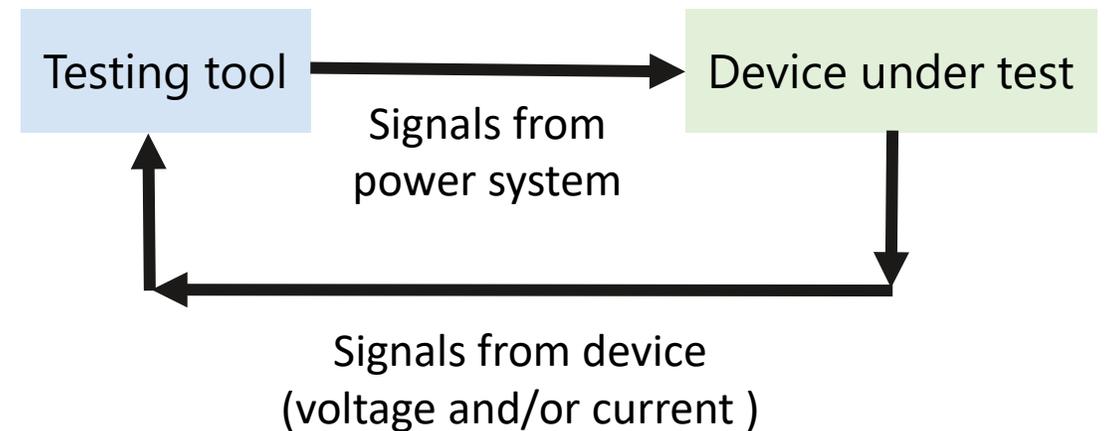
Open Loop vs Closed Loop PHIL

- Some applications might consider open loop as PHIL
- Challenges comes from closing the loop for kW to MW range
- All further discussions are referring to [Closed Loop](#) PHIL

Open Loop



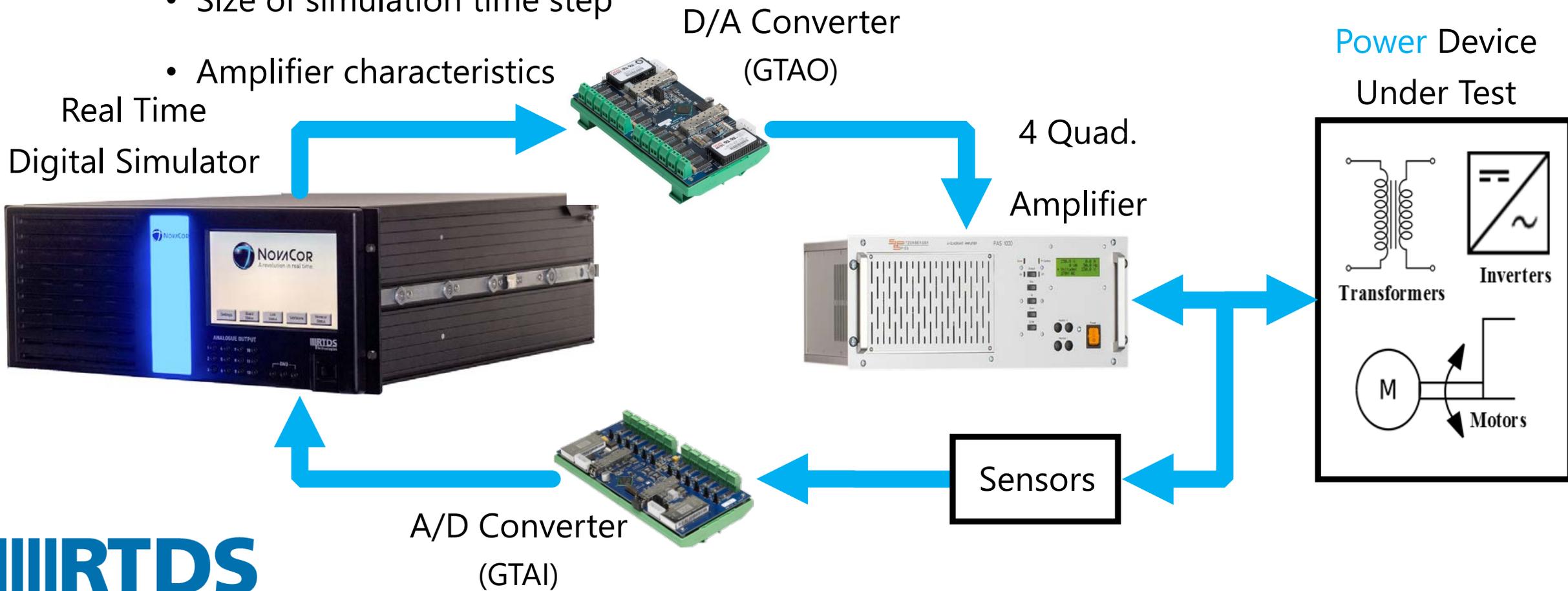
Closed Loop





Key Factors for PHIL Simulation

- Delays in the PHIL interface affect simulation accuracy and stability
- Size of simulation time step
- Amplifier characteristics





Recent Developments

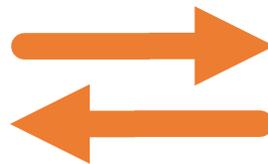
- **Aurora Interface**

- Digital link between RTDS™ and Spitzenberger & Spies Amplifiers
- Reduced loop delay & noise
- Improved stability and accuracy

Real Time
Digital Simulator



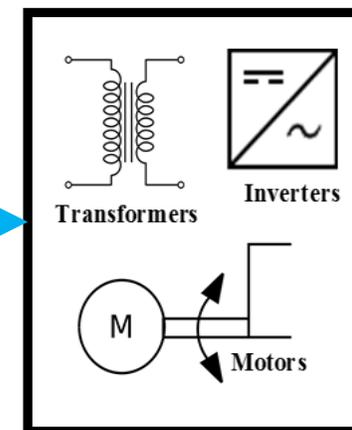
Aurora
Interface



4 Quad.
Amplifier



Power Device
Under Test

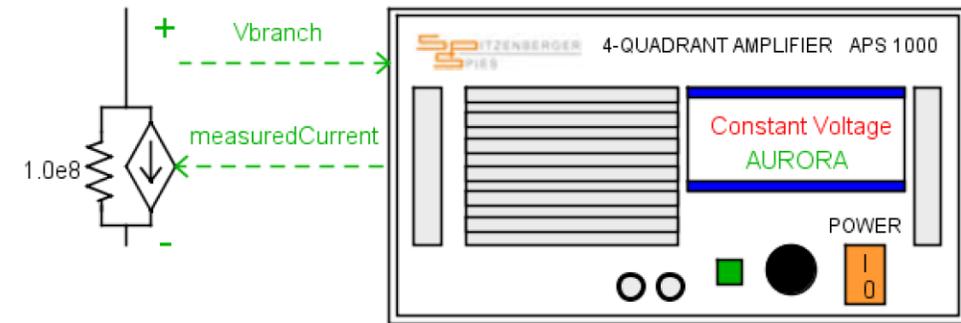




Recent Developments

- SPS Aurora Component

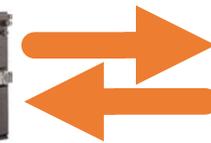
- Aurora link and voltage/current source embedded into a single component
- Positioning of voltage/current interfacing sources can be reversed
- Optimized timing for data exchanges to further reduce loop delay
- Automatic or user defined scaling factors for over 12 SPS amplifier models
- User controlled feedback switched for open/closed loop operation
- Embedded CRC32 checksum for error detection during data exchanges



NovaCor™ Real Time Digital Simulator



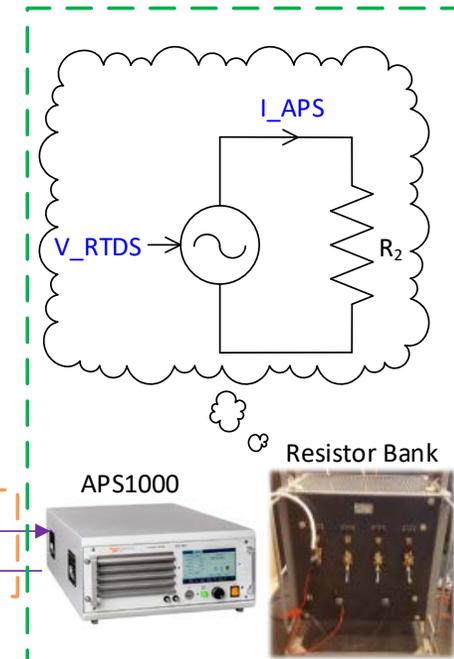
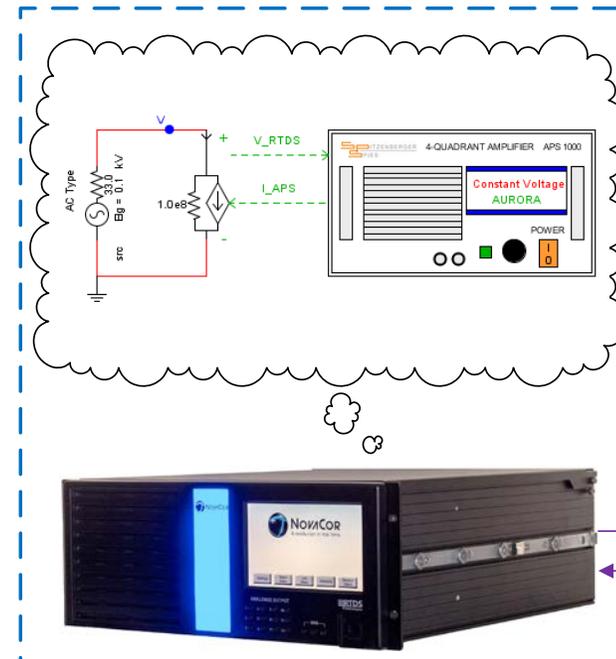
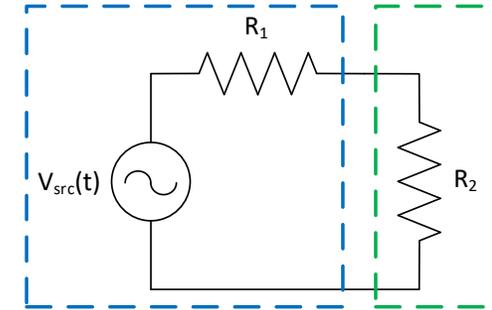
Aurora Interface





Recent Developments

- Example: Voltage Divider with Aurora Interface
- Voltage source and source resistor on simulation side of PHIL interface
- Load resistor on amplifier side of interface
- From the perspective of the RTDS, voltage out, current in
- User configurable measurements delay and filter within SPS amplifier



Aurora Link

V_RTDS

I_APS

APS1000

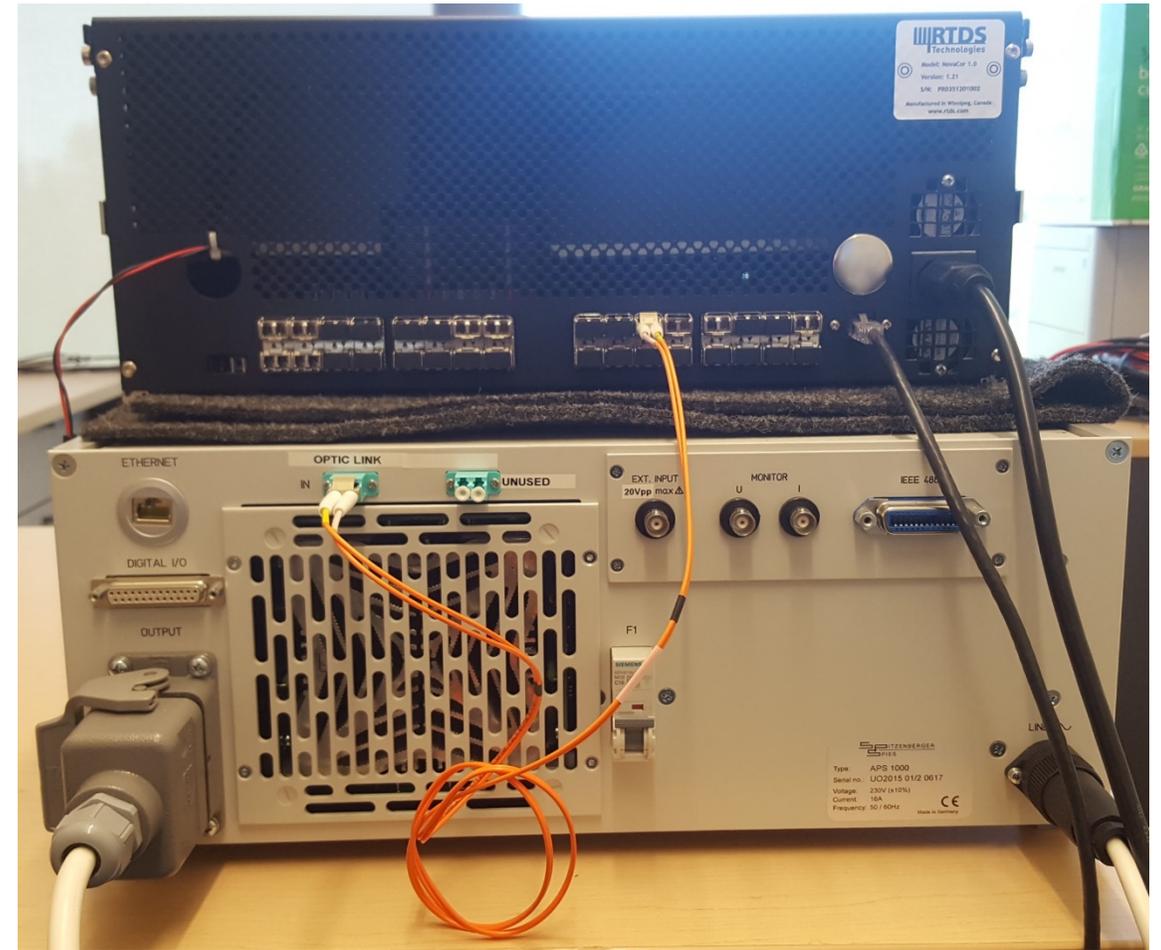


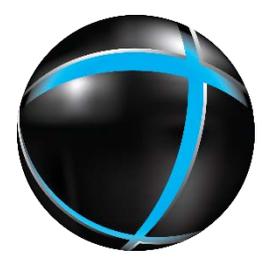
Resistor Bank



Recent Developments

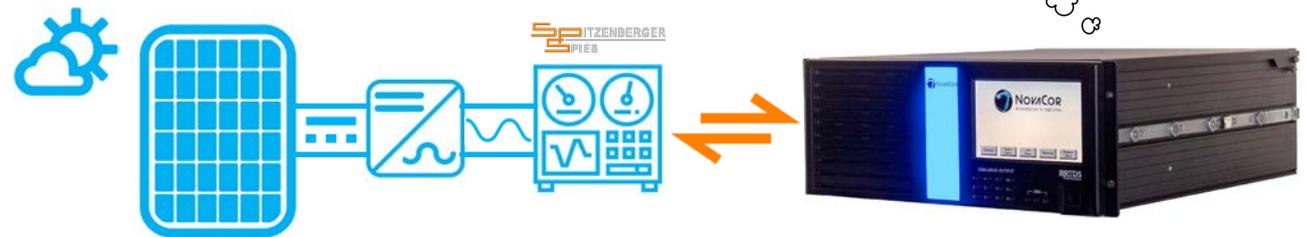
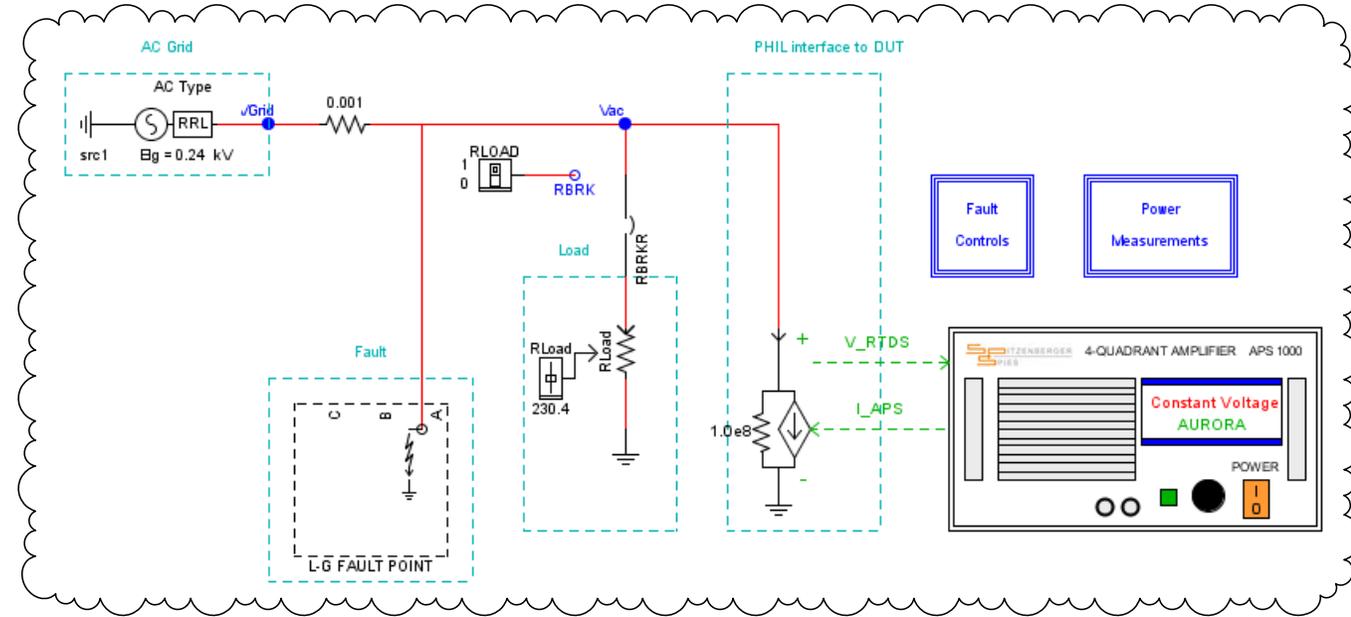
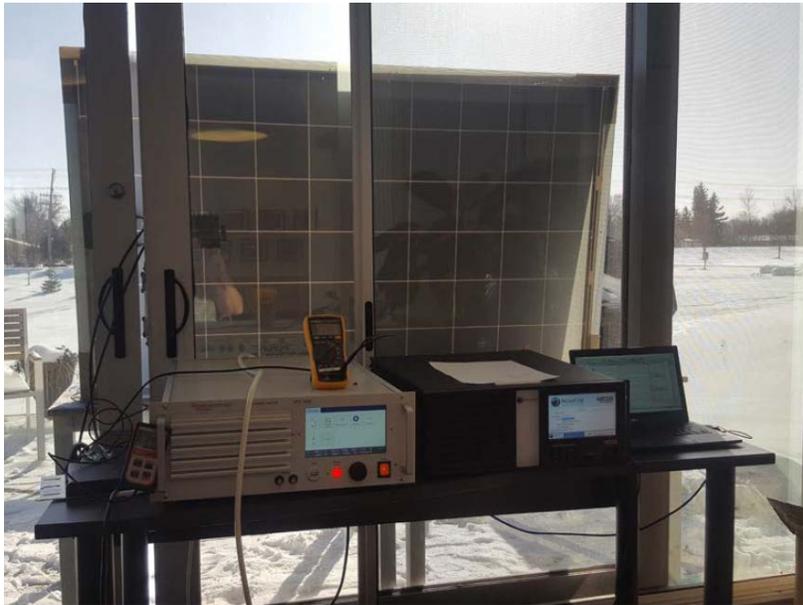
- Example: Voltage Divider with Aurora Interface
- Hardware Connections for Aurora Interface
- Requires a licensed Aurora Port on either PB5 or NovaCor based RTDS™
- Eliminates use of Analog Output/Input cards in PHIL interface
- Simplifies wiring and eliminates possibility of user error when wiring





Recent Developments

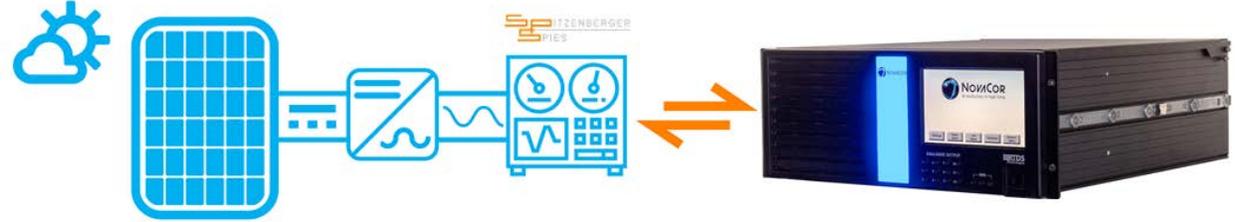
- Example: PV Panel & Micro Inverter
- 255W PV Panel
- 225W Microinverter



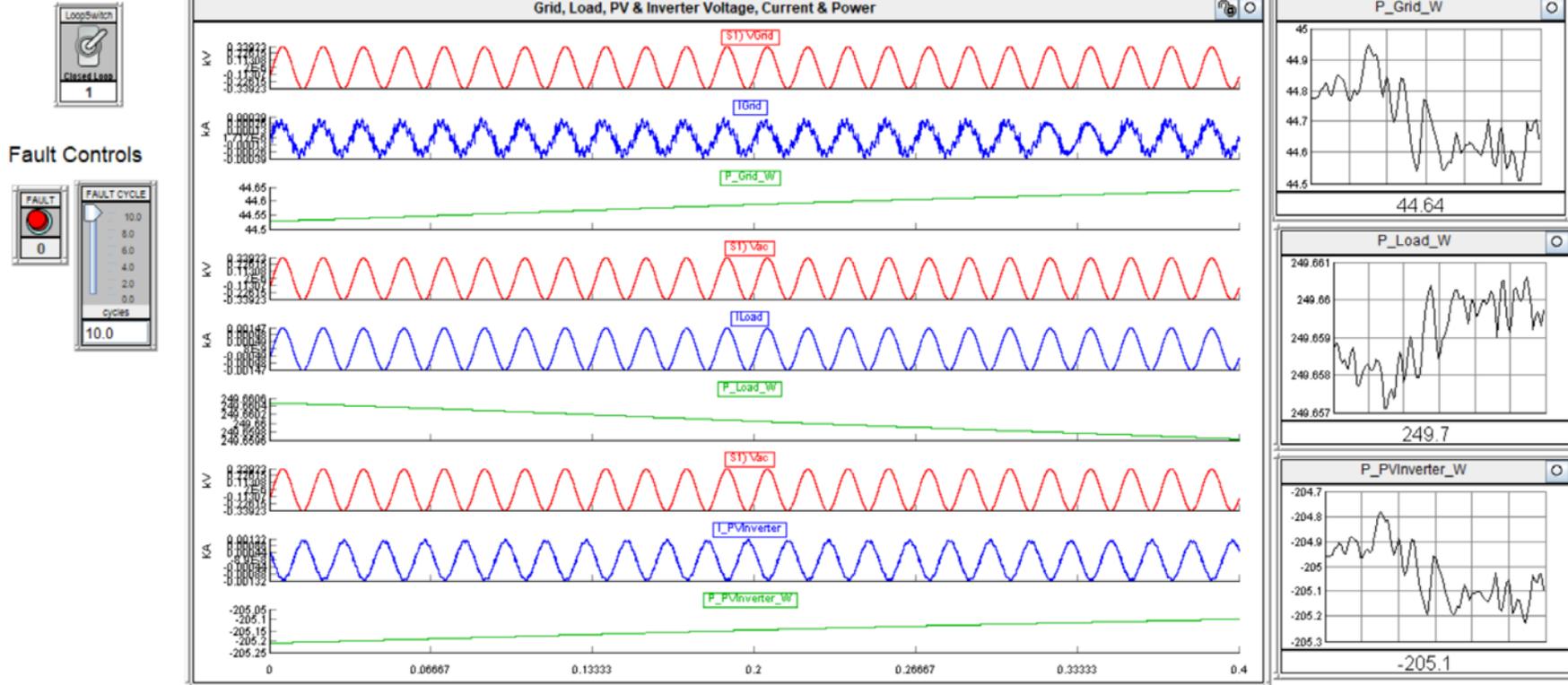


Recent Developments

- Example: PV Panel & Micro Inverter
- 250W Load
- 45W from simulated AC grid
- 205W from PHIL PV panel & microinverter



Feedback Loop - Open or Closed





Conclusions

- Aurora interface offers improved accuracy and stability due to newly developed component models
- PHIL Report documenting our experiences
 - Freely Available on our website ([https://www.rtds.com/wp-content/uploads/2015/12/RTDS PHIL Report-2.pdf](https://www.rtds.com/wp-content/uploads/2015/12/RTDS_PHIL_Report-2.pdf))
 - Discusses key factors for PHIL simulation
 - Interface Algorithms
 - 4 Quadrant Amplifiers
 - Characterizing PHIL Interface
 - Stability and Accuracy of PHIL Interface
 - PHIL Applications (e.g. PV Panel & Microinverter)

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Power Hardware In the Loop Simulation (PHIL)

The diagram illustrates the PHIL setup. A computer rack on the left is connected via a circular arrow to a power amplifier unit in the center. This amplifier is connected to a set of electrical components on the right, including a transformer, a motor, a solar panel, and a battery. The background of the diagram features three vertical panels: a dam, a power substation, and a wind farm.



Questions?