CHILplug: an integrated CHIL interface

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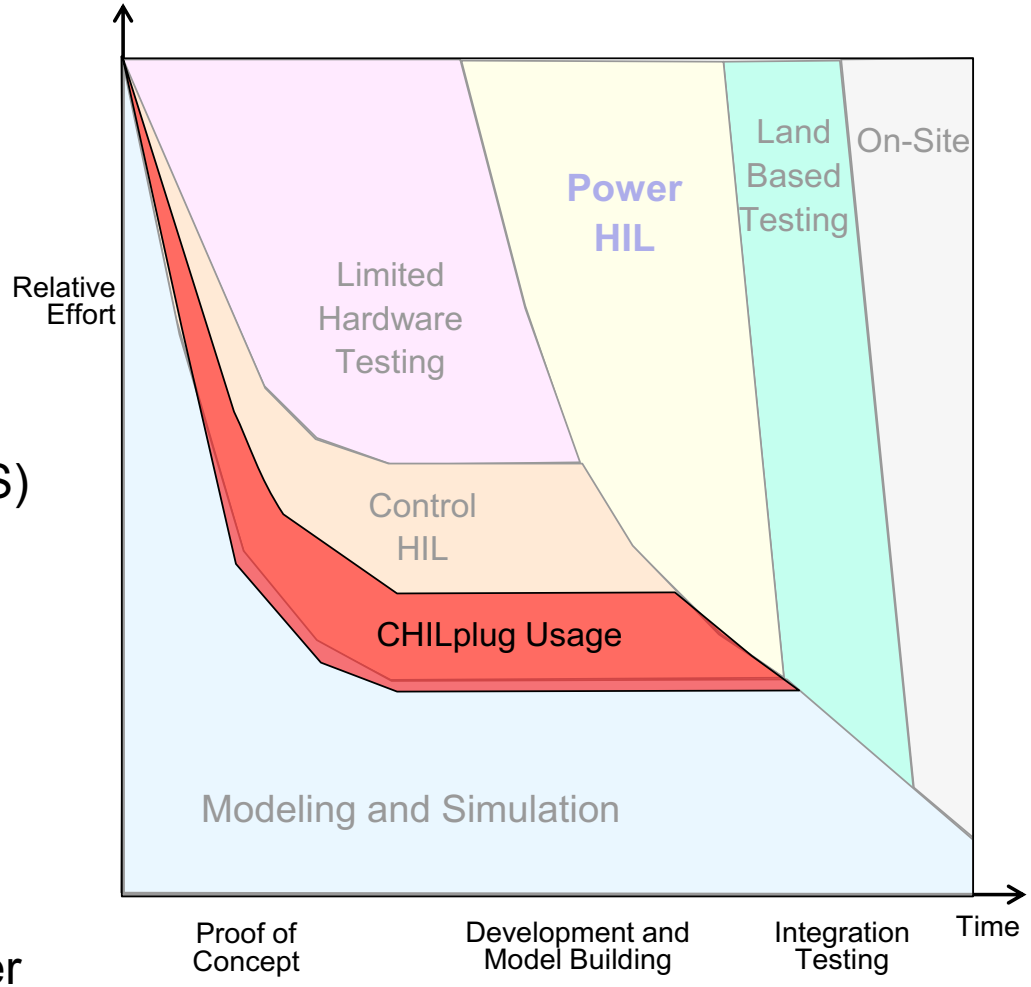
Outline

- Introduction
- CHILplug concept
- GADTAMS: MV-scale SiC Converter
- First CHILplug implementation
- Multi -- CHIL integration
- PHIL -- CHILplug as multi-purpose tool
- Conclusions

Introduction

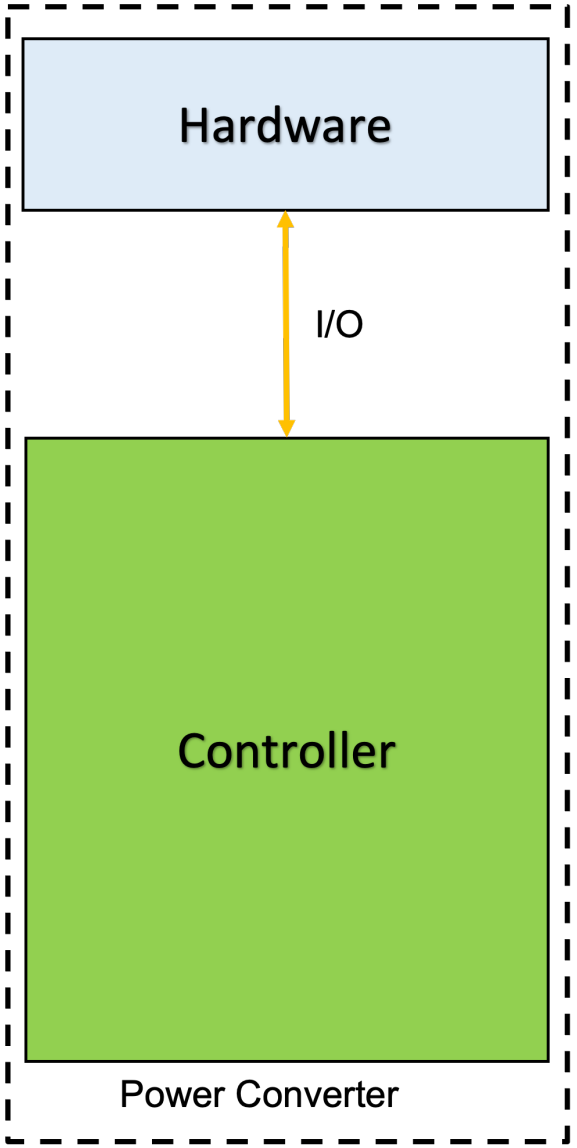
- Power electronic converter (PEC) controllers
  - Rapidly changing requirements for PECs
  - PEC controller is likely to receive upgrades over its operating life
- Controller-hardware-in-the-loop (CHIL) test
  - Commonly used in development process
  - De-risk testing of controller using a real-time simulator (RTS)
- CHIL challenges
  - Requires signal conditioning to interface controller I/O with RTS
  - Limited number of signals going to/from the controller
  - Modifies PEC connection to controller
- A need for…
  - CHIL interface (the CHILplug) integrated with PEC controller
  - Facilitates development and testing of controller over PEC lifetime



Potential CHILplug usage during the design and development process

The CHILplug

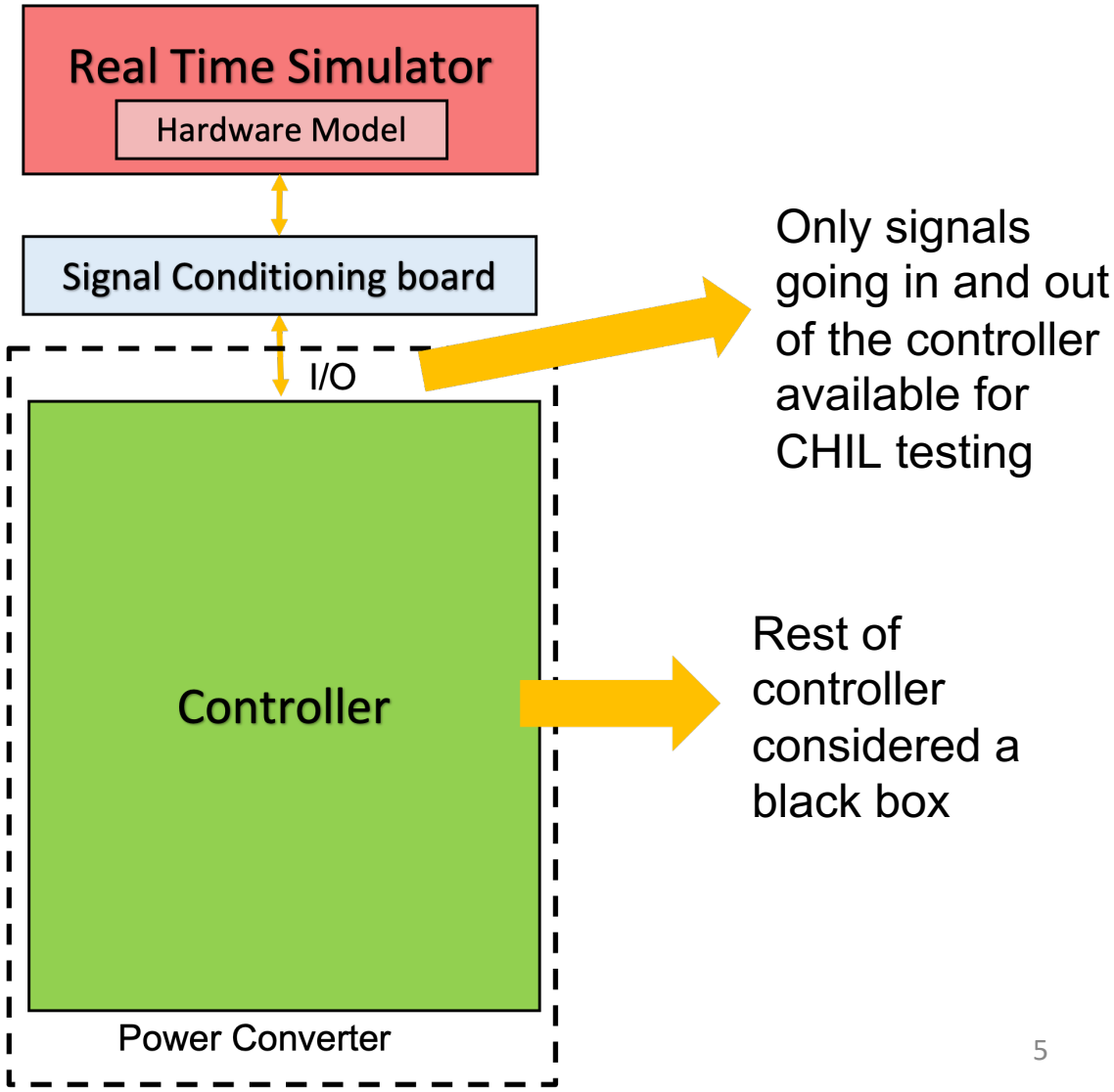
PEC Hardware Connection



The CHILplug

PEC Traditional CHIL

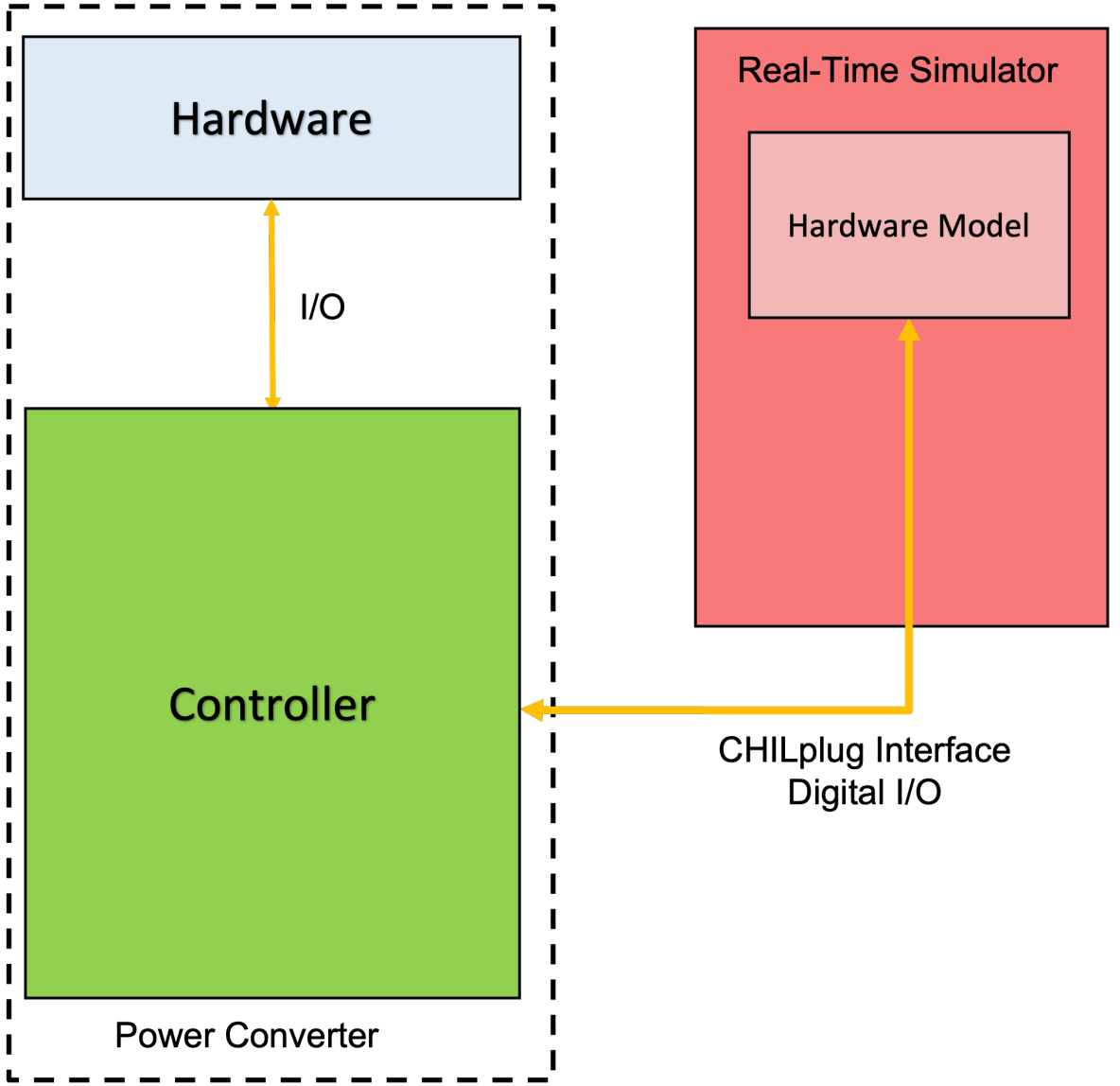
- Traditional CHIL
  - Different signal conditioning
  - Dedicated CHIL setup



The CHILplug

PEC CHILplug

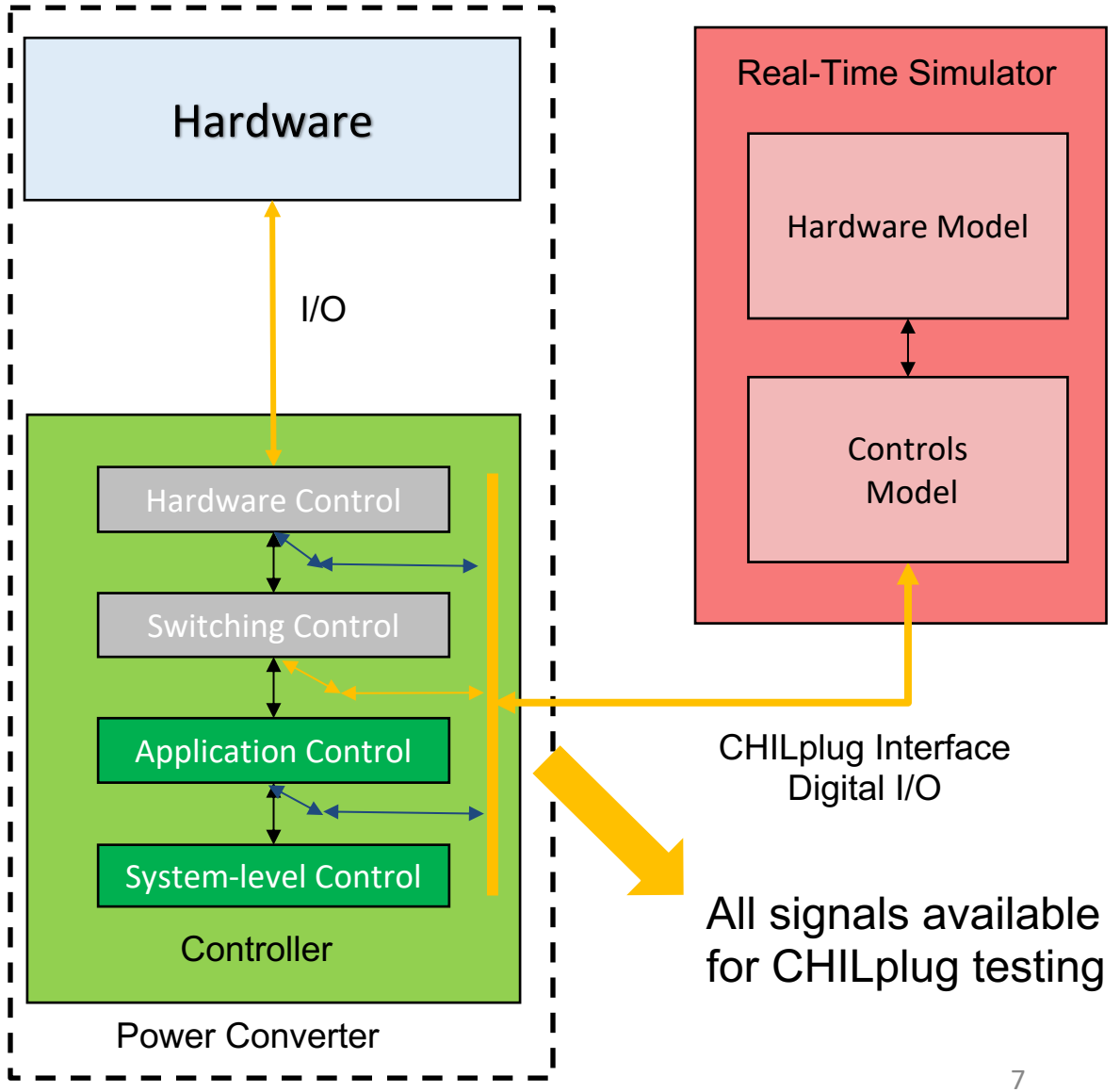
- The CHILplug concept
  - Dedicated computer network to/from RTS
    - Avoids analog signal processing



The CHILplug

PEC CHILplug

- Testing with the CHILplug
  - Software plug between PEC controller layers
  - All CHIL required data over one communication channel
- CHILplug challenges
  - Controller needs digital I/O capable of high-speed communication
  - No existing standard for testing
- U.S. Patent US11016452B2 (2021)

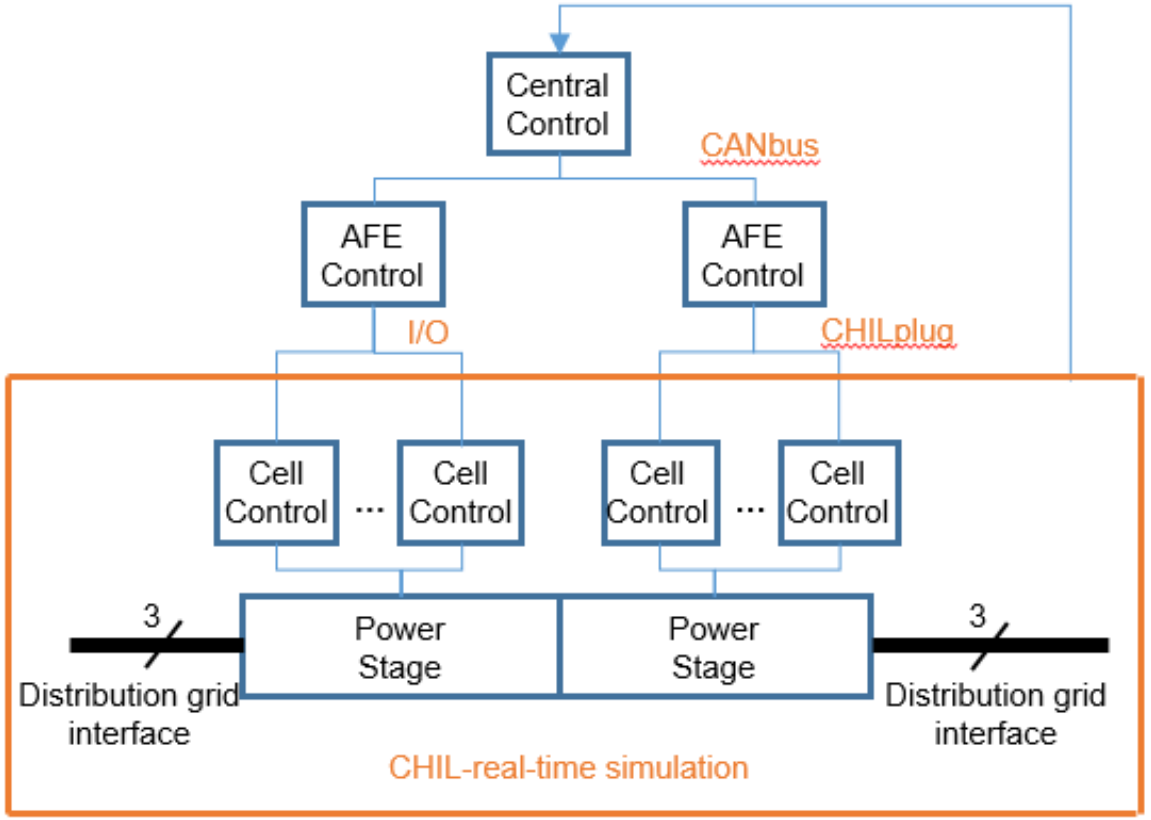


GADTAMS: MV-scale SiC Converter Development and System Integration

- NREL – Project lead, grid analysis, ESIF testbed for 10 kV SiC MVB2B
- OSU – MMC AFE, CHIL, power stage testing, single-phase 13.8 kV/20 kVdc
- FSU – SC-MMC AFE, Y-Matrix modulation, CHIL and PHIL testing, single-phase 13.8 kV/20 kVdc

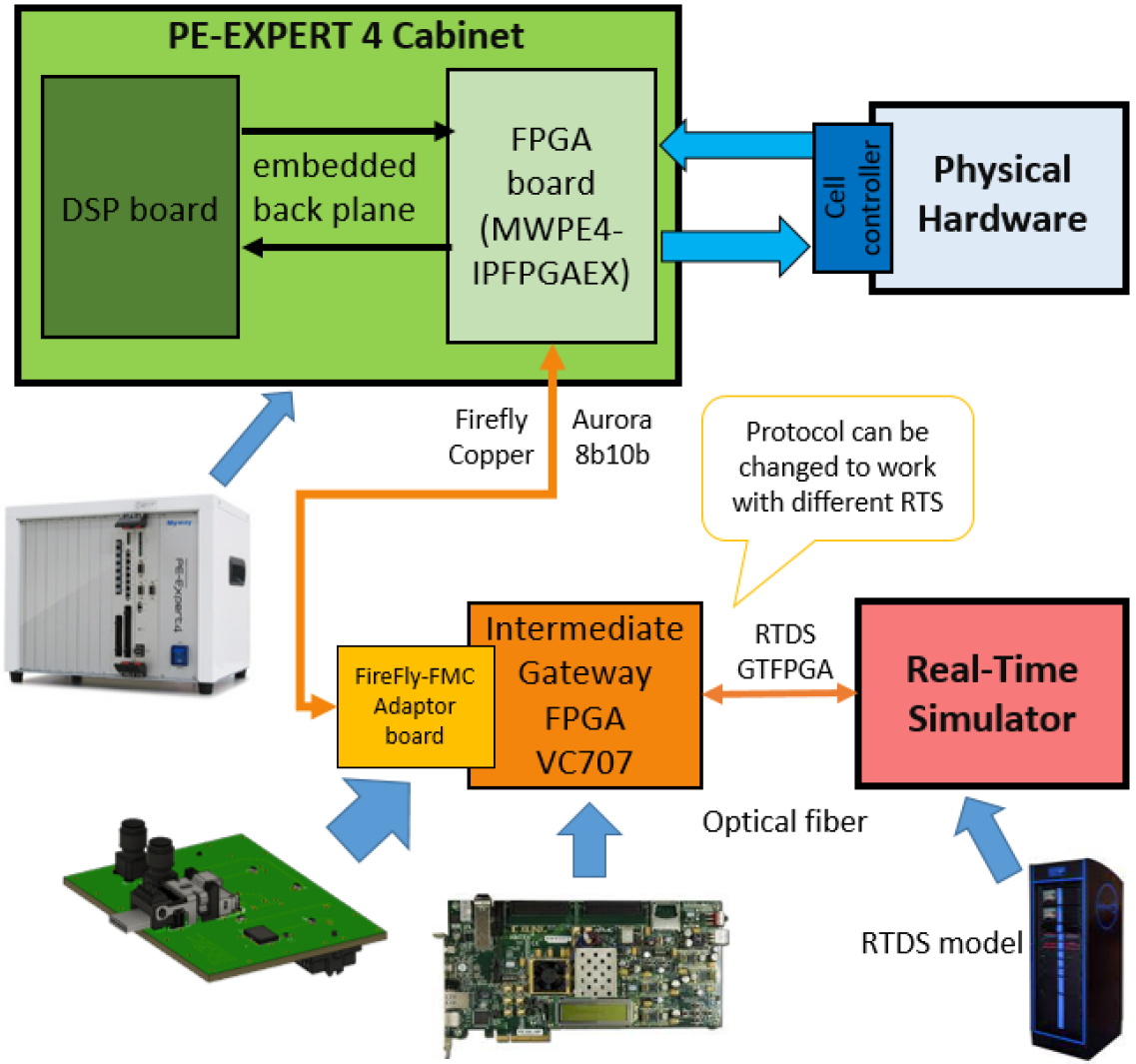
NREL
NATIONAL RENEWABLE ENERGY LABORATORY

- Build & test 4.16 kVac – 8 kVdc SiC converter
- Develop the “CHIL-plug” idea
- PHIL-based demonstration of 4.16 kV capability



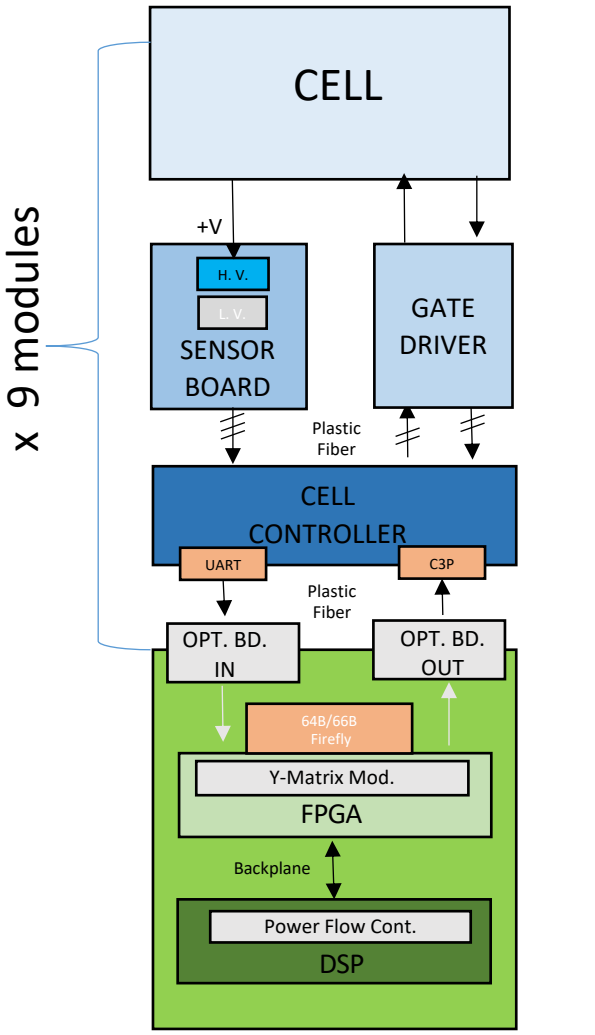
First CHILplug Implementation

- Switched-Capacitor Modular Multilevel Converter (SiC-MMC) Project
  - PE-Expert controller:
    - DSP board: Converter & Application control layers
    - FPGA board: Switching control layer
- CHILplug requirements
  - CHILplug interface at FPGA to be able to connect to switching control layer
- CHILplug interface implementation
  - Available FPGA connection not compatible with RTS
  - Intermediate gateway needed to communicate with RTS

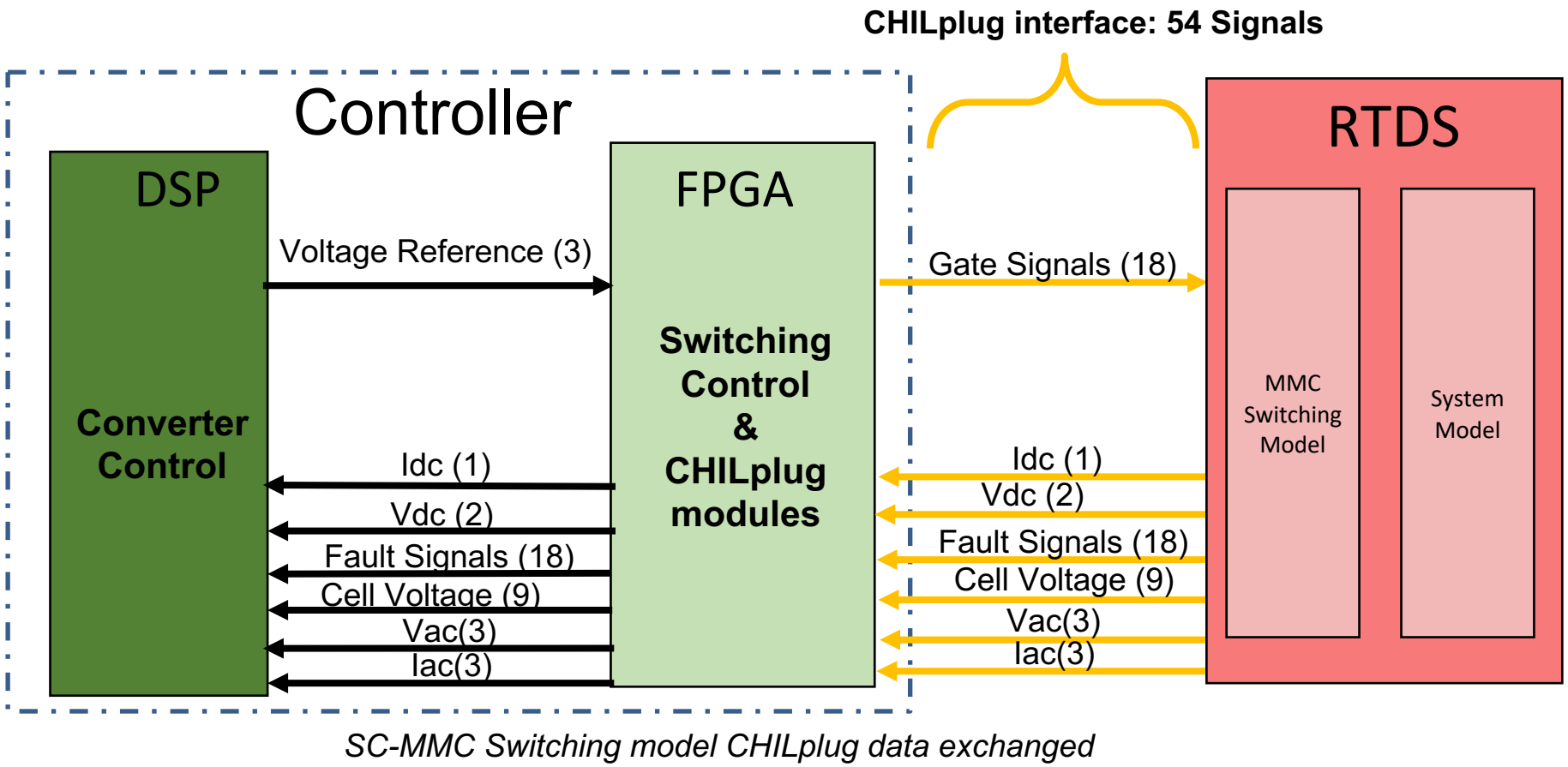


Current work

- Medium voltage 3-phase SC-MMC-based dc-ac converter
  - Controller validation: Average model &Switching model

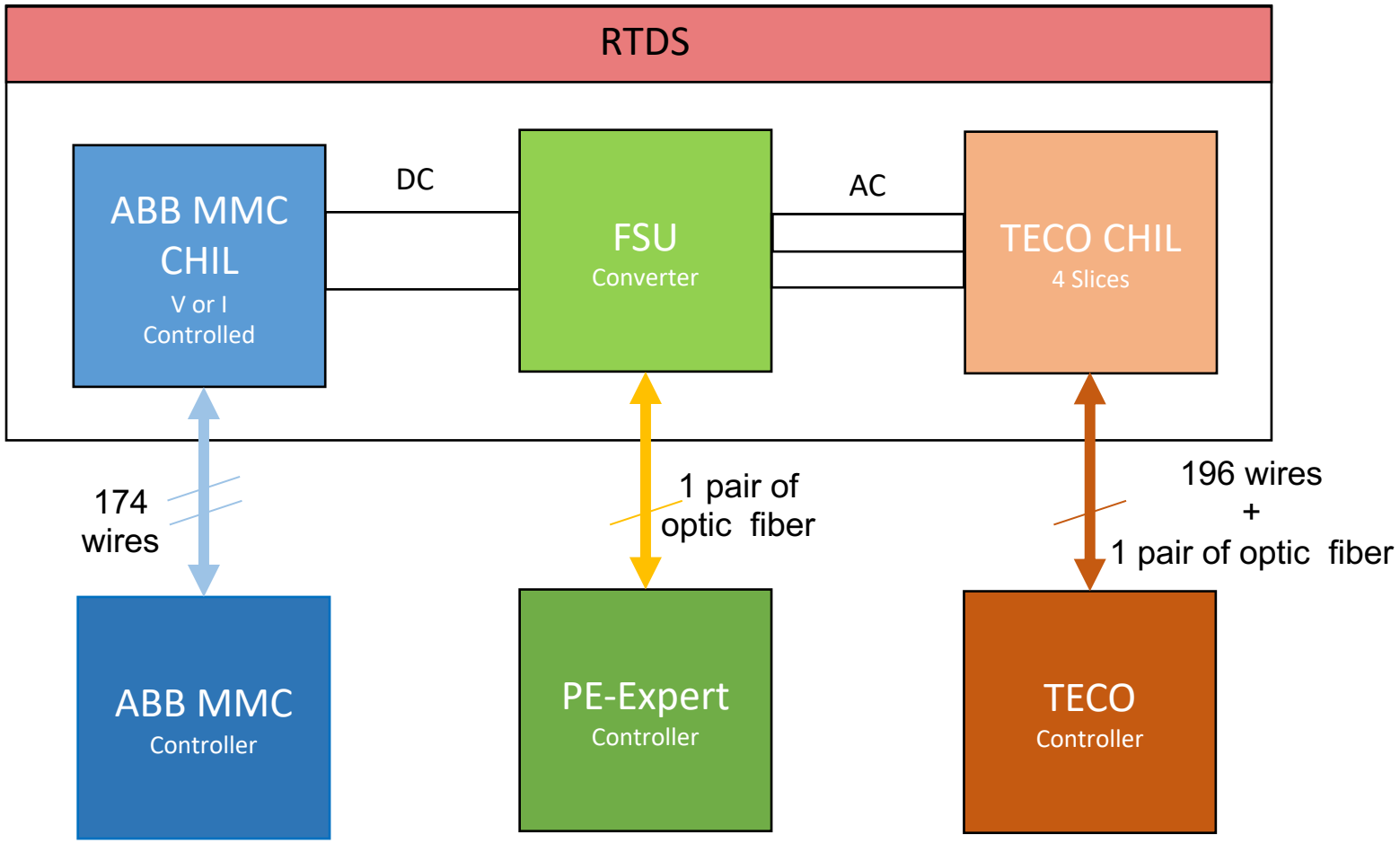


SC-MMC Hardware diagram



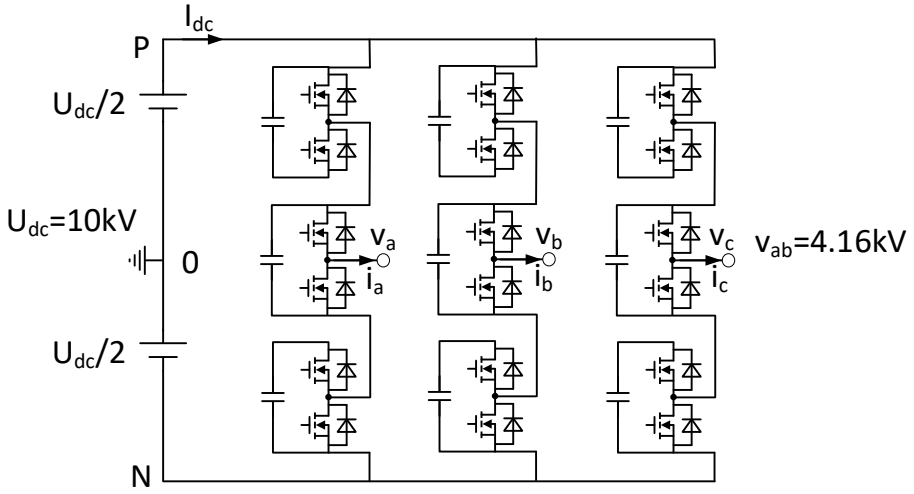
SC-MMC Switching model CHILplug data exchanged

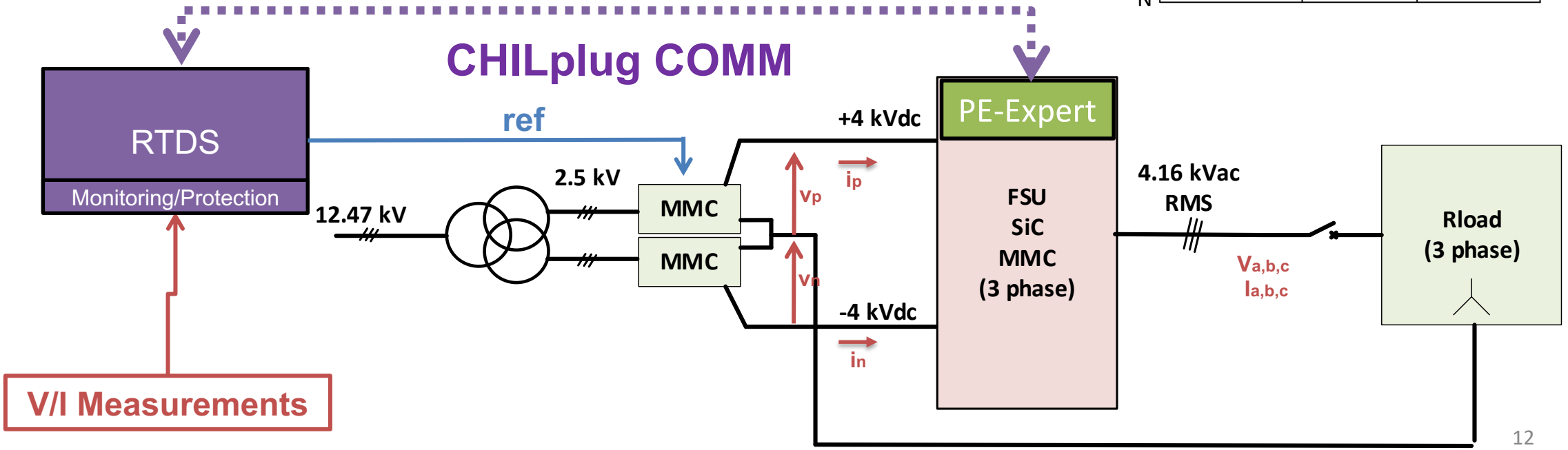
Integrated CHIL



The CHILplug as a recording tool

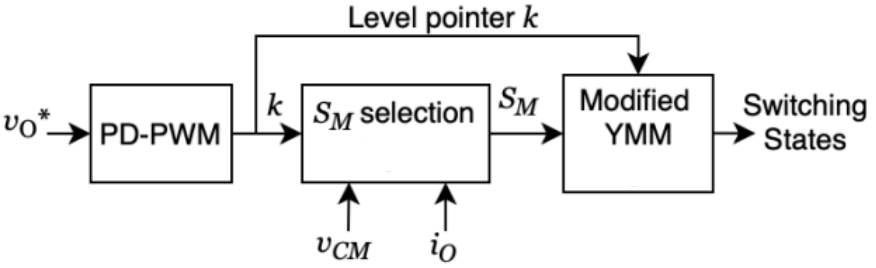
- **Hardware test for 3 phase 4.16kV**
  - The CHILplug used as an auxiliary channel in test to monitor and log data
    - In situ monitoring of
      - Measured data going to the controller
      - Controller internal signals
  - Data recorded using RTS timesteps

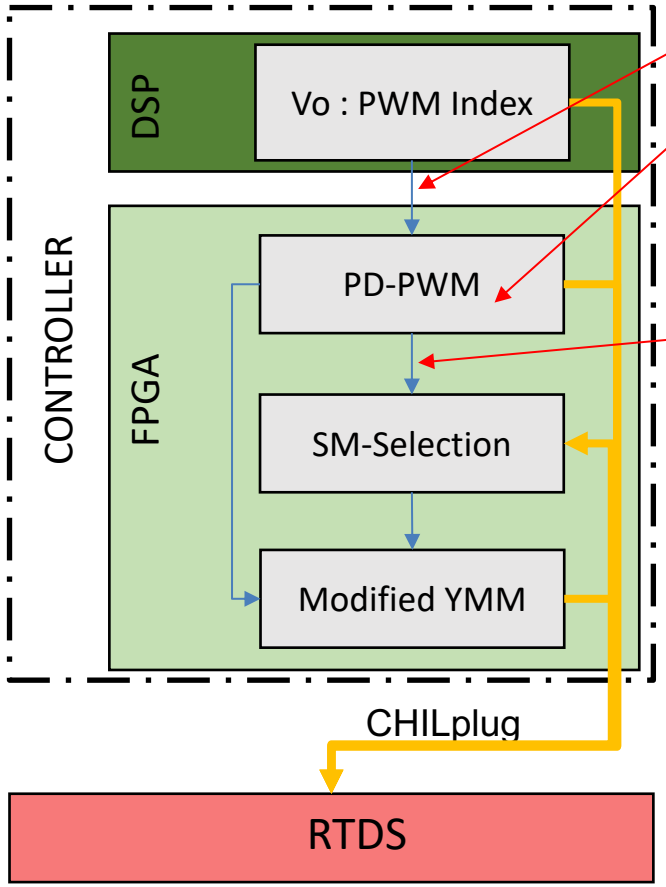


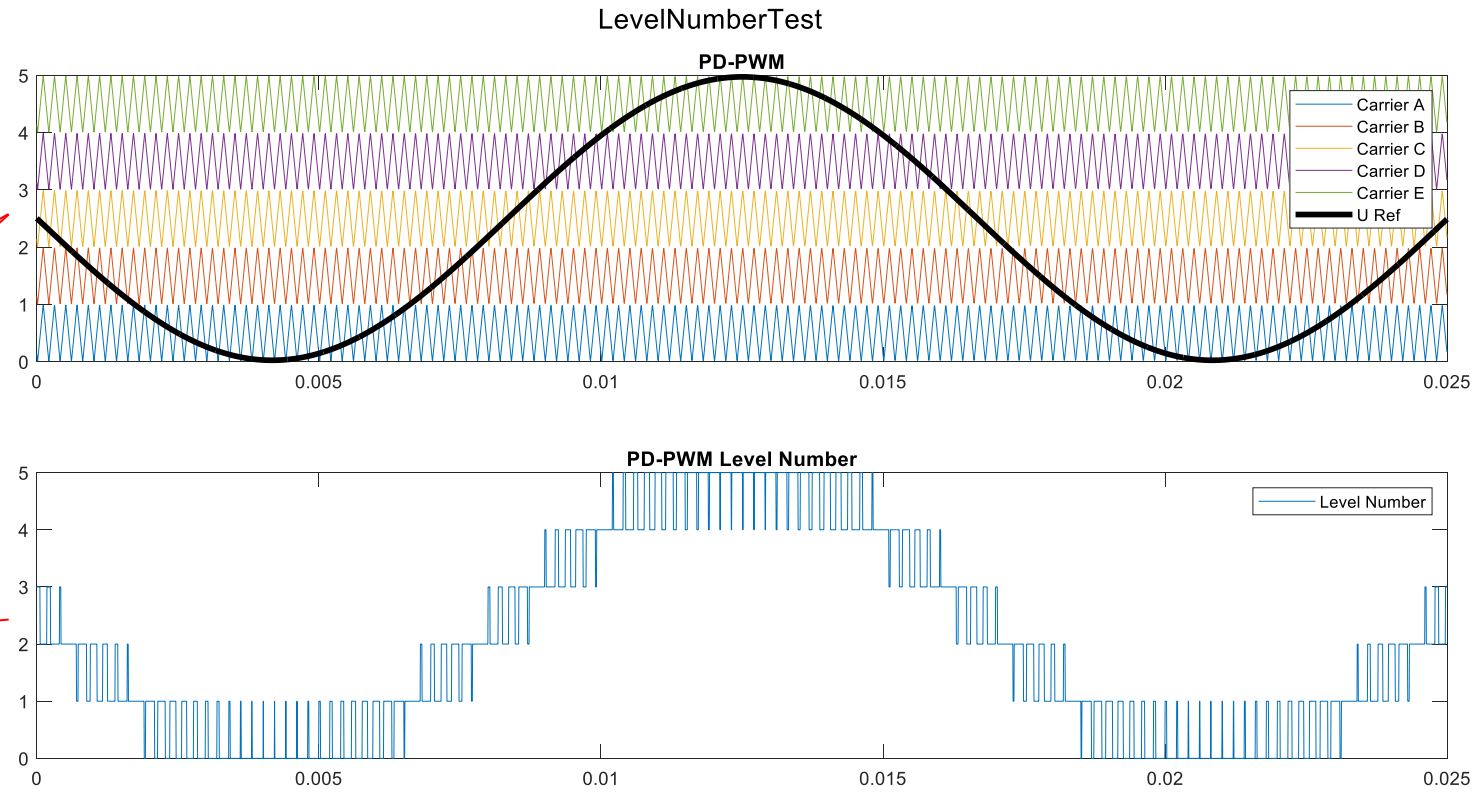


SC-MMC 3 Phase 4.16 kV Hardware test diagram

CHILplug use case : Modulation test



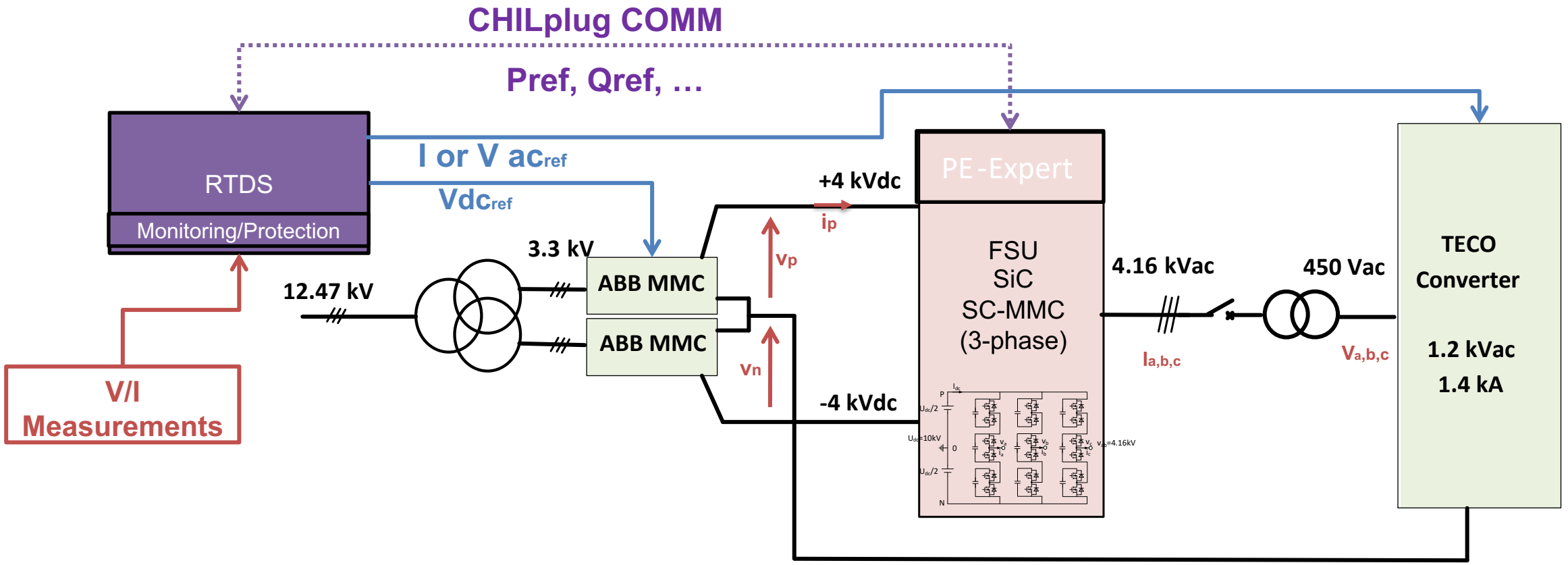




Ability to monitor signals not available in traditional CHIL

R. B. Gonzatti, Q. Yang, H. Pourgharibshahi and F. Peng, "Switched Capacitor MMC Submodule Voltage Balancing with Reduced Number of Voltage Sensors," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 4342-4348, doi: 10.1109/ECCE44975.2020.9235703.

CHILplug: multi-purpose tool:
Operation and recording



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Conclusion

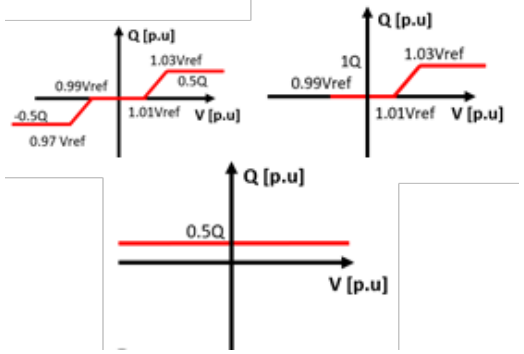
- CHILplug concept
  - Convenient PEC control interface to RTS
  - Facilitates transition between offline and CHIL development stages
  - Reduces complexities in setting up a CHIL environment
  - Requires consideration in early stages of design (controller selection)
- Additional benefits
  - Additional high-speed interface available through all development stages for verifying algorithms and recording data
- Usefulness
  - CHILplug physical interface (and future standardization) avoids costly one-off solutions
- Future work
  - Hardware validation of control scheme of a medium voltage 3-phase SC-MMC-based dc-ac converter using average and switching models and hardware results

Converter development -- Testing

HIL setups

- Different configurations to parallel development stages including
  - Single leg (full voltage)
  - 3-phase full and reduced voltage
- Testing steps during control implementation to derisk
- System-level testing of converters
  - Grid-emulation to allow testing
    - Basic operation
    - Advanced control modes (e.g., active-reactive power based on IEEE 1547 options)
    - Abnormal conditions (protection including ride-through and trip events)

Operation with distribution grid conditions



IEEE 1547-derived testing scenarios