6TH INTERNATIONAL WORKSHOP ON GRID SIMULATOR TESTING OF WIND TURBINE POWER TRAINS AND OTHER RENEWABLE TECHNOLOGIES

# Gain Scheduling Control Design for Active Front End for PHIL Application: an LMI Approach

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# Outline

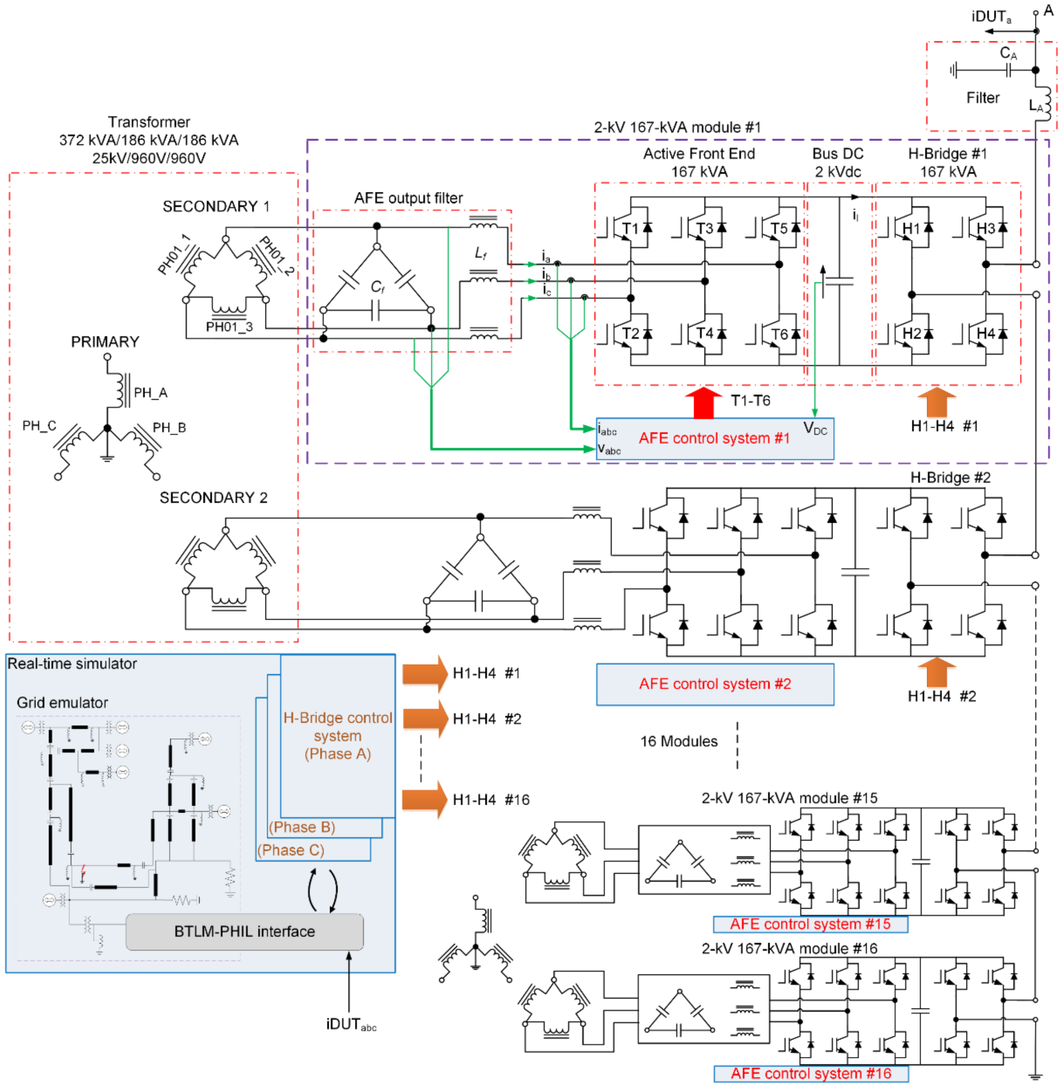
# Introduction

- **Context: develop a PHIL infrastructure at IREQ**
  - Enabling elements: 25 kV distribution test line and commercial real time simulation software HYPERSIM
- **Majority of elements are designed and developed at IREQ – more flexibility and better performance**
- **Several R&D challenges associated with such an approach:**
  - Hardware design and optimization
  - **Inverter control design**
  - PHIL interface design

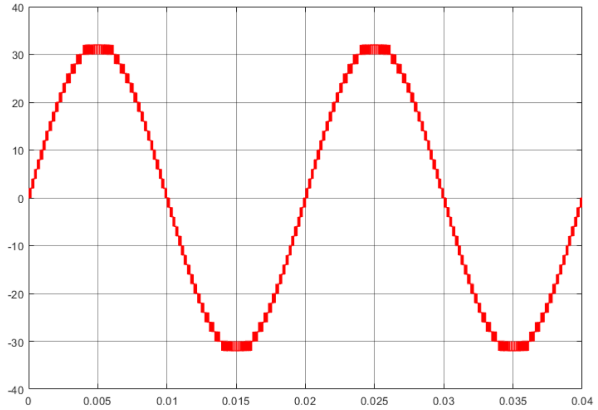
# Inverter topology

- **25-kV 3-phase power amplifier**
- **16 cascaded H-bridges per phase connected in series**
- **Each H-bridge is powered by an isolated 3-phase two-level AC-DC grid-connected inverter (Active Front End, AFE)**
- **2-kV, 167-kVA module – AFE (including output filter) with associated DC link and H-bridge**

# Inverter topology



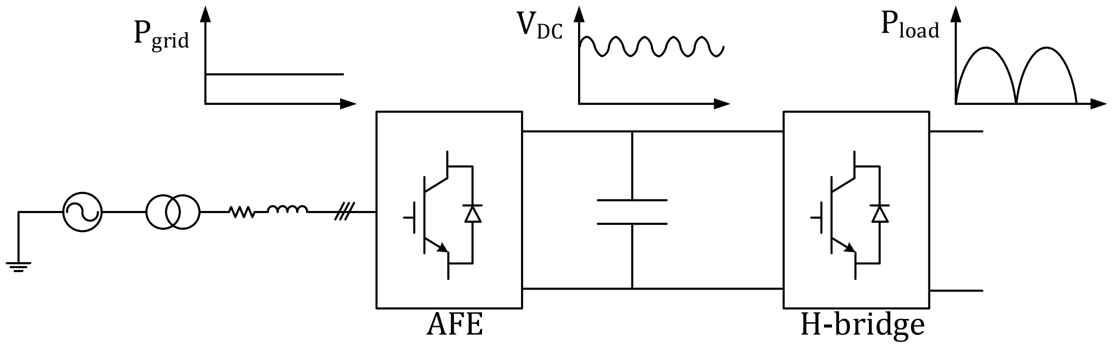

- **Transformerless AC output – allows for DC and low frequency components in the generated voltage**
- **High quality of the output voltage waveform – smaller AC filter**




- **Independent control of each phase – capable of reproducing unbalanced conditions**

# AFE control design challenge

- **AFE control objective: tight regulation of DC link voltage (2 kV) – requires aggressive controller**
- **Each module performs AC-DC-AC conversion between 3-phase and single-phase system -> pulsating power and DC link voltage ripple with** $2 \times f_{AC}$




- **Aggressive DC voltage control reacts to DC voltage ripple -> grid output current distortion**
- $f_{AC}$ **can change – applying filters is difficult**

# AFE control design challenge

- **How to ensure fast DC link voltage regulation without distorting grid current for various frequencies of the synthesized AC voltage?**

# Proposed solution

- **Allow for the DC link voltage ripple, but reduce the amplitude by oversizing the DC link capacitor**
- **For 60 Hz the resulting ripple amplitude is less than 1% of the nominal DC voltage**
- **Controller architecture: <u>gain scheduling</u> <u>full state feedback</u> control**

# Proposed solution

- **Gain scheduling**
  - Two sets of voltage regulator gains for fast and slow control
  - Fast control objective: quickly bring DC link voltage within the specified bandwidth (1%) during transient (tolerate grid current distortion)
  - Slow control objective: minimize the grid current distortion in steady state
  - Scheduling variable - DC link voltage (may change fast and is not generally constant in steady state)

# Proposed solution

- **Full state feedback**
  - Simple formulation as an optimal control problem (minimize closed loop system norms)
  - Semidefinite Programming program (SDP) formulation – convex problem with a linear objective and Linear Matrix Inequality (LMI) constraints: numerically tractable
  - Allows for a straightforward bumpless transfer strategy
  - Requires an appropriate model for controller design
- **Inner current/outer voltage control loops**
  - Allows for limiting the grid current
  - Sequential design (a series of convex problems to solve)

# Model development

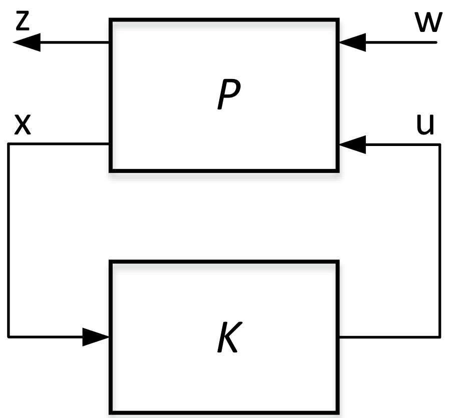
- Available measurements: transformer secondary voltage, DC link voltage and AC output filter current
- Full state feedback requires a model for which available measurements are states (or states can be easily deduced)
- Third order model comprising dq-frame RL filter current dynamics and DC link voltage
- For robust tracking, augment the model with the integrals of states we want to track (currents and voltages)

# Model development

- **Perform change of variables to introduce state deviations**
- **Assumptions**
  - Inverter is lossless
  - Ignore output filter capacitor
  - Ignore PLL and abc-to-dq transformation
  - Ignore anti-aliasing filter (AAF)
- **Nonlinear model – linearize around an operating point (which one to choose?)**

# Controller design

- **Formulate the problem of current/voltage control design as an optimal control problem**




- **Find the (static) gain K that minimizes the norm of the transfer function matrix between w (disturbance vector) and z (performance vector)**

# Controller design

- **SDP formulation to minimize the $H_\infty$-norm:**

$$\underset{Y,M}{\text{minimize}} \quad \gamma$$

$$Y > 0$$

$$\begin{bmatrix} AY + B_u M + (AY + B_u M)^T & B_w & (CY + D_u M)^T \\ B_w^T & -\gamma I & D_w^T \\ CY + D_u M & D_w & -\gamma I \end{bmatrix} < 0$$

- **To achieve the desired dynamic response**
  - introduce weights in the performance vector
  - add constraints (e.g., bound the $H_2$-norm of the transfer function between load current and voltage regulator output for slow control)

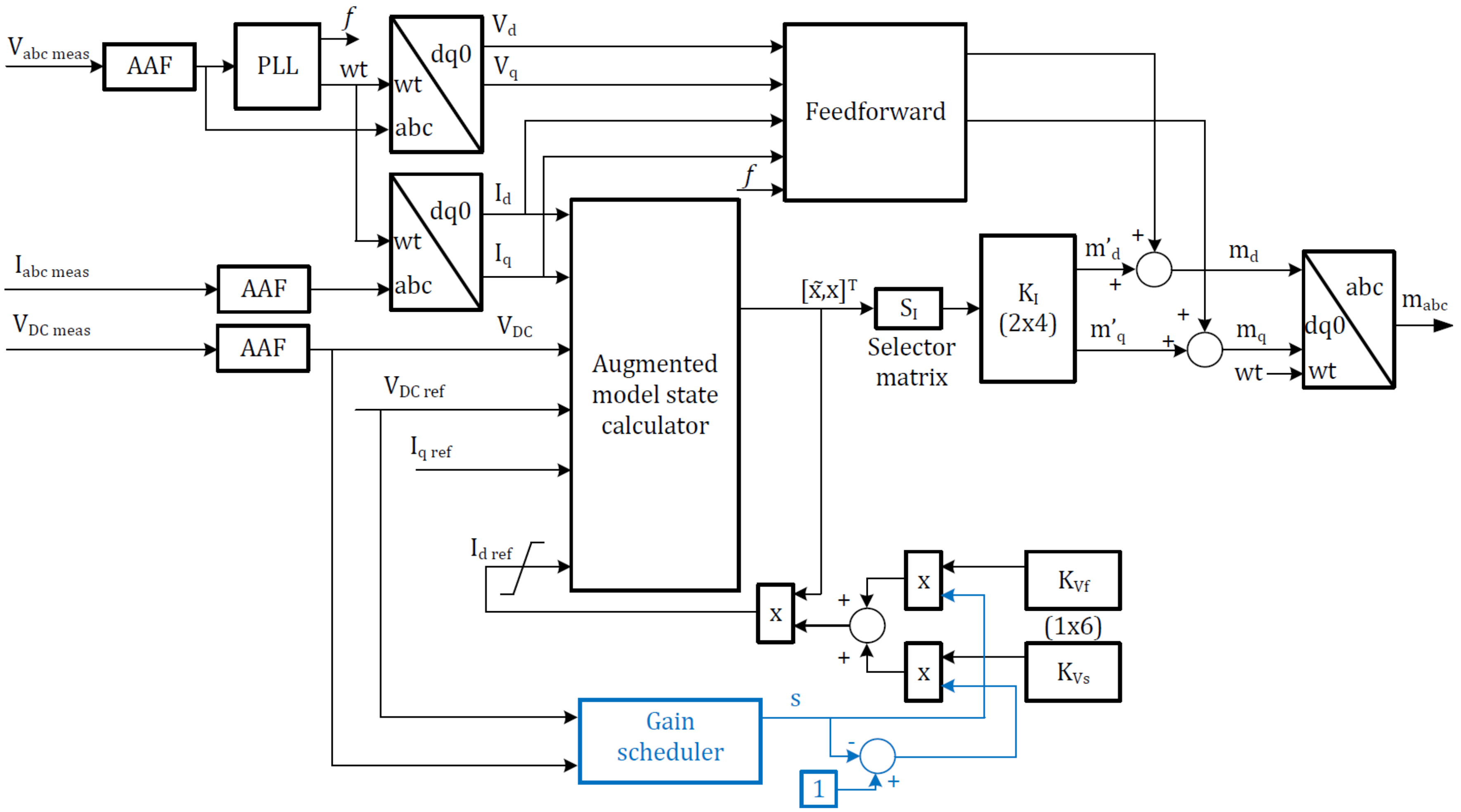
# Controller design

- **Design of inner current control (find $K_I$)**
  - Introduce feedforward to accelerate regulation and decouple d- and q-axis dynamics
  - Simplify the model – assume constant DC link voltage (AFE model is linear in this case!)
  - Actual topology returned by the SDP solver is that of a PI control
- **Design of outer voltage control (find $K_{Vs}$ and $K_{Vf}$)**
  - Current regulator in closed loop for the design of outer voltage control
  - Adapt optimization formulation to reflect control objectives
  - Non-minimum-phase system in inverting mode of operation (power to grid)
  - Available controller bandwidth is reduced
  - Linearize and design voltage control for inverting mode to have sufficient stability margins

# Controller design

- **Bumpless transfer: how to switch between fast and slow gains without undue transients caused by controller output discontinuities?**
  - Generally requires controller conditioning
- **For static feedback, simple strategy can be applied**
  - Gains of the augmented states (integral states) should be placed before the integrator
  - Form the convex combination of both controllers: $K_V = sK_{Vf} + (1-s)\,K_{Vs}, \quad 0 \leq s \leq 1.$
  - Change $s$ to achieve desired gain transfer performance

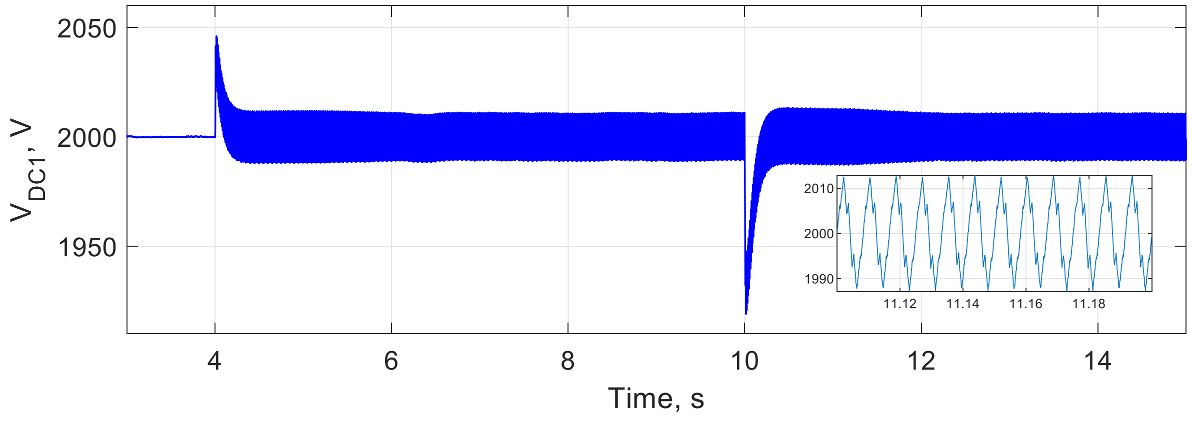
# Controller design

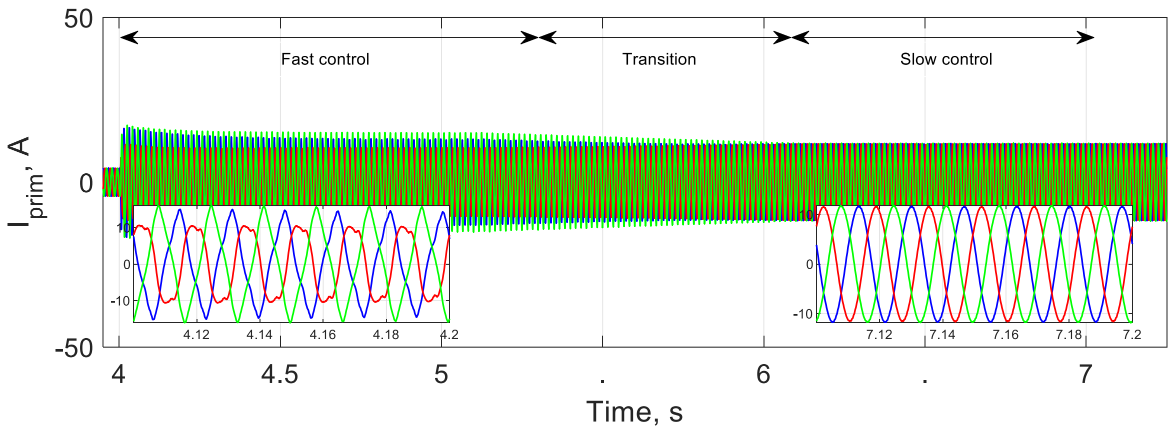


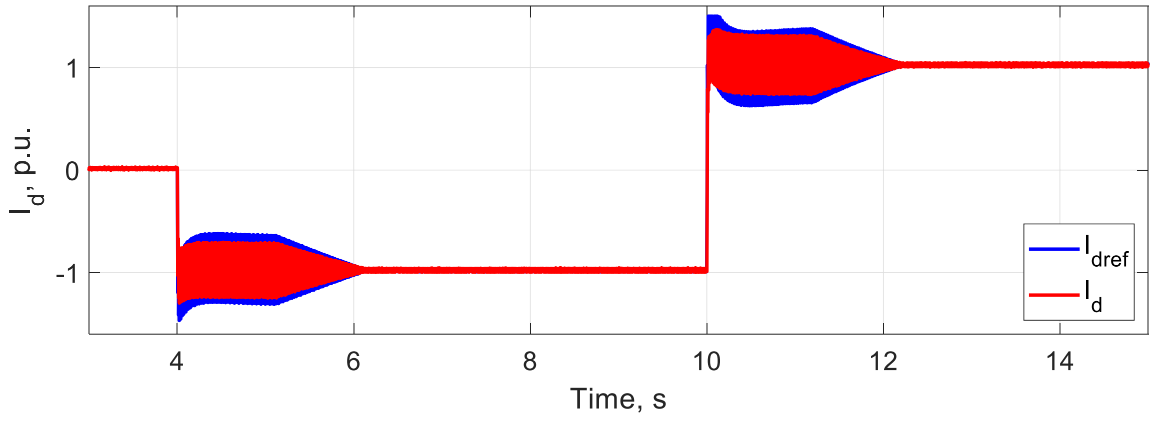
# Test results: Offline simulations

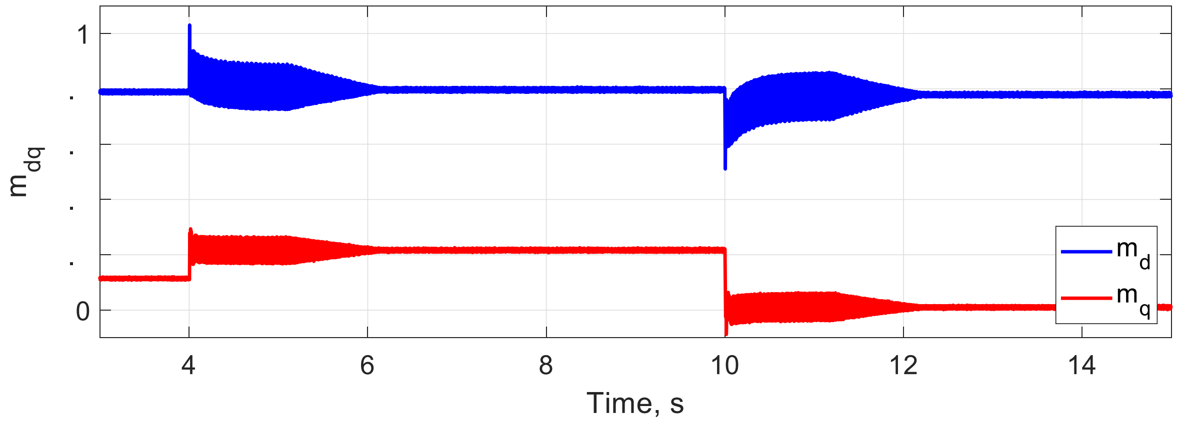
- **Simulink model of two modules in parallel**
  - Impact of modeling assumptions
  - Impact of phase-shifted PWM to reduce current harmonics
  - Interactions between AFEs connected to the same transformer
- **Matrix representation of 3-winding transformer**
  - Parameters derived from lab tests
- **Constant current AC load**
  - Change load current direction to change from inverting to rectifying mode of operation

# Test results: Offline simulations



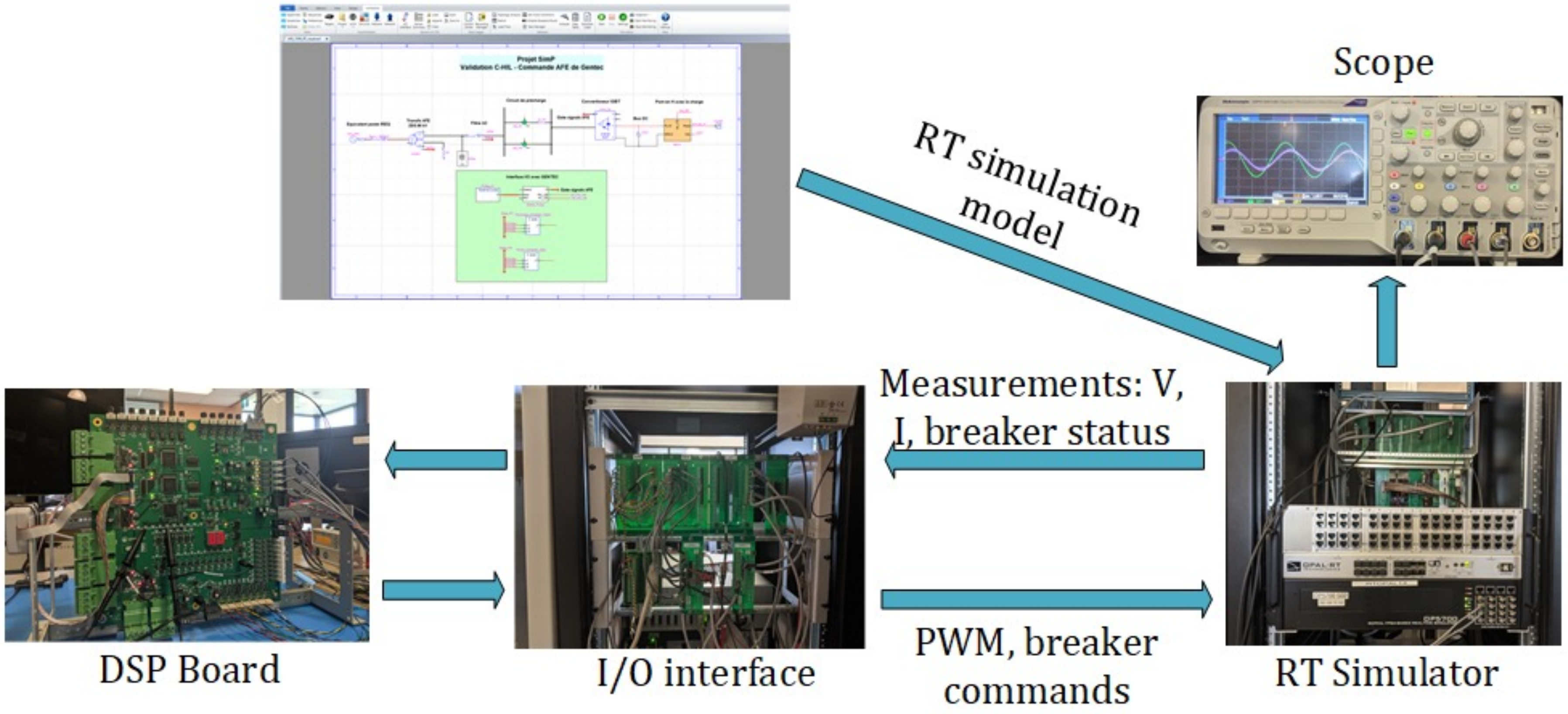



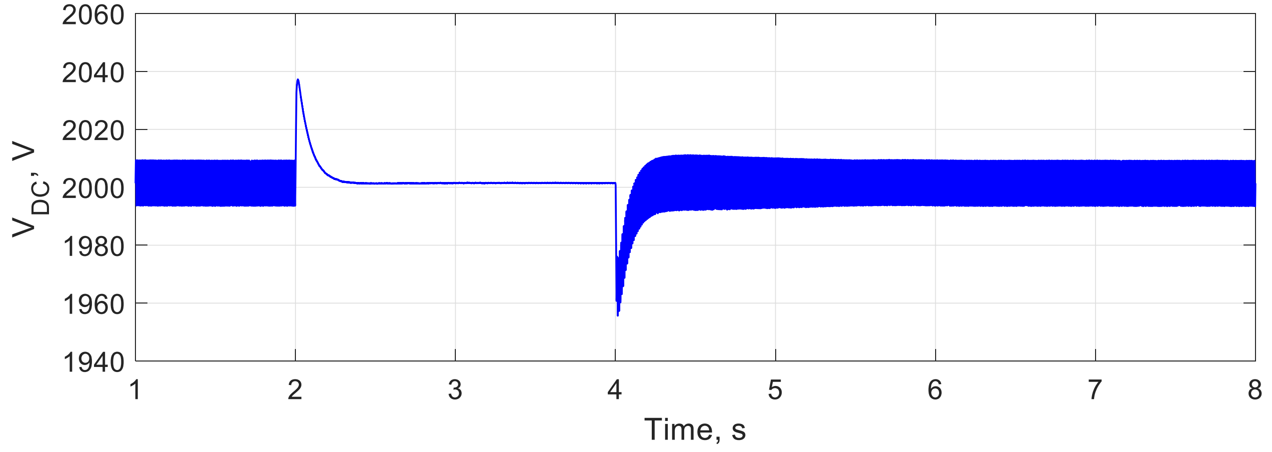
# Test results: Real-time simulations

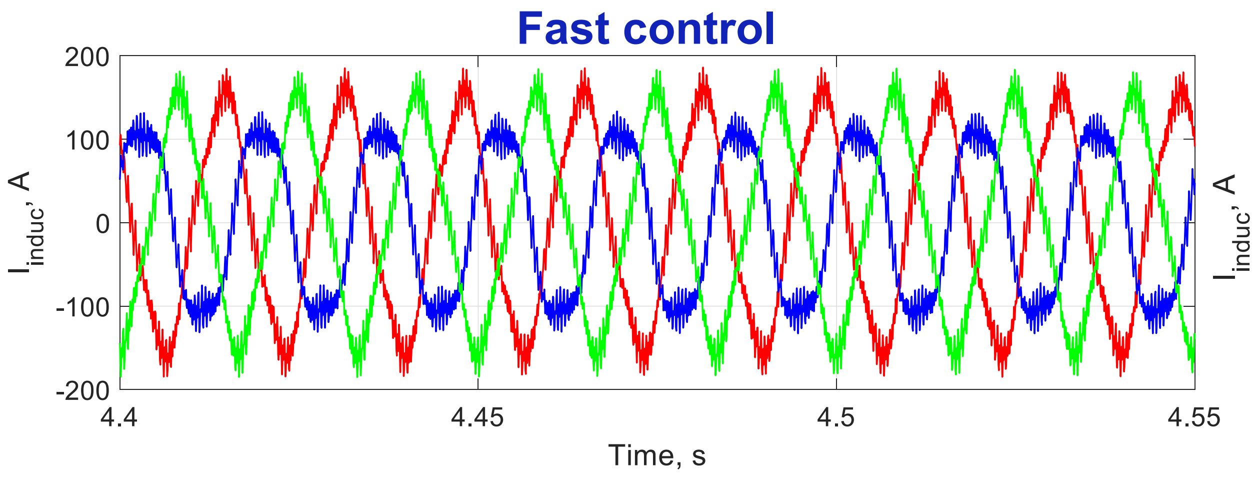
- **Real-time AFE modeling in Hypersim using switching functions (simulation time step of 25 us)**
  - The equivalent of sixteen H-bridges is simulated
  - Resulting DC current divided by the number of H-bridge modules is injected as the load current of the AFE
- **Custom-made DSP board to execute the compiled code of the controller (execution time step of 250 us)**
- **State machine to include additional control and protection functions, including startup sequence**
- **Resistive load drop/pickup are simulated**

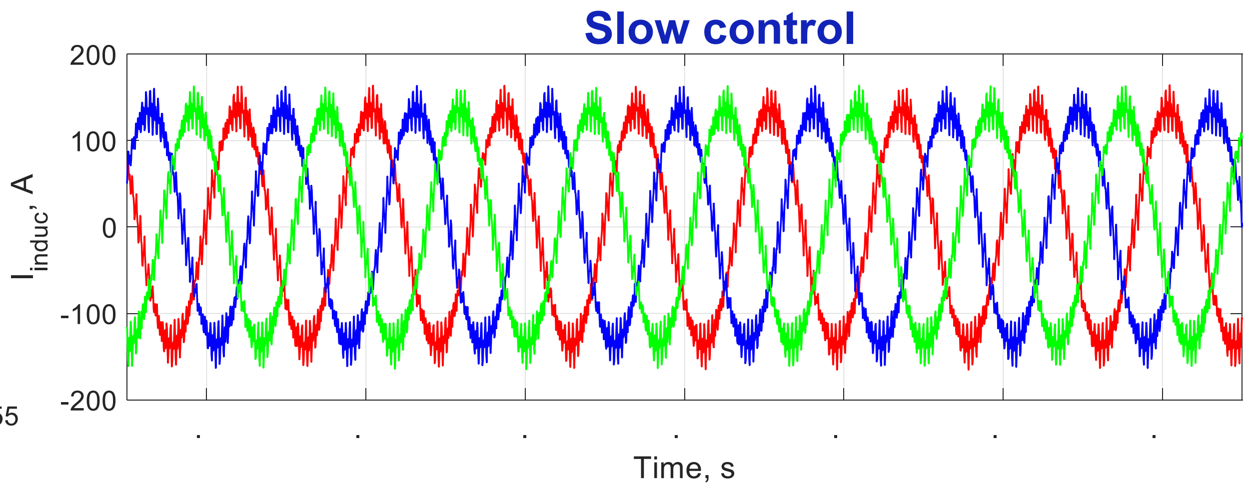
# Test results: Real-time simulations



# Test results: Real-time simulations



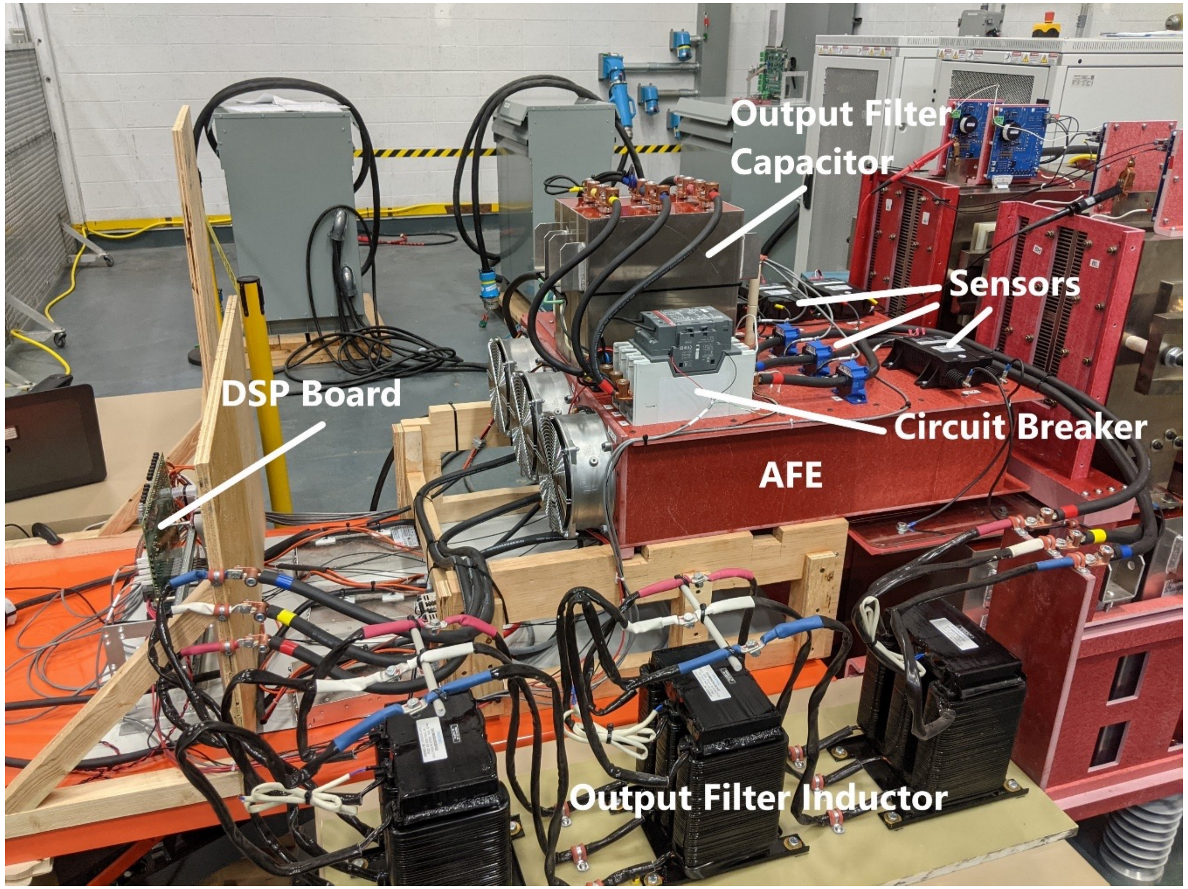



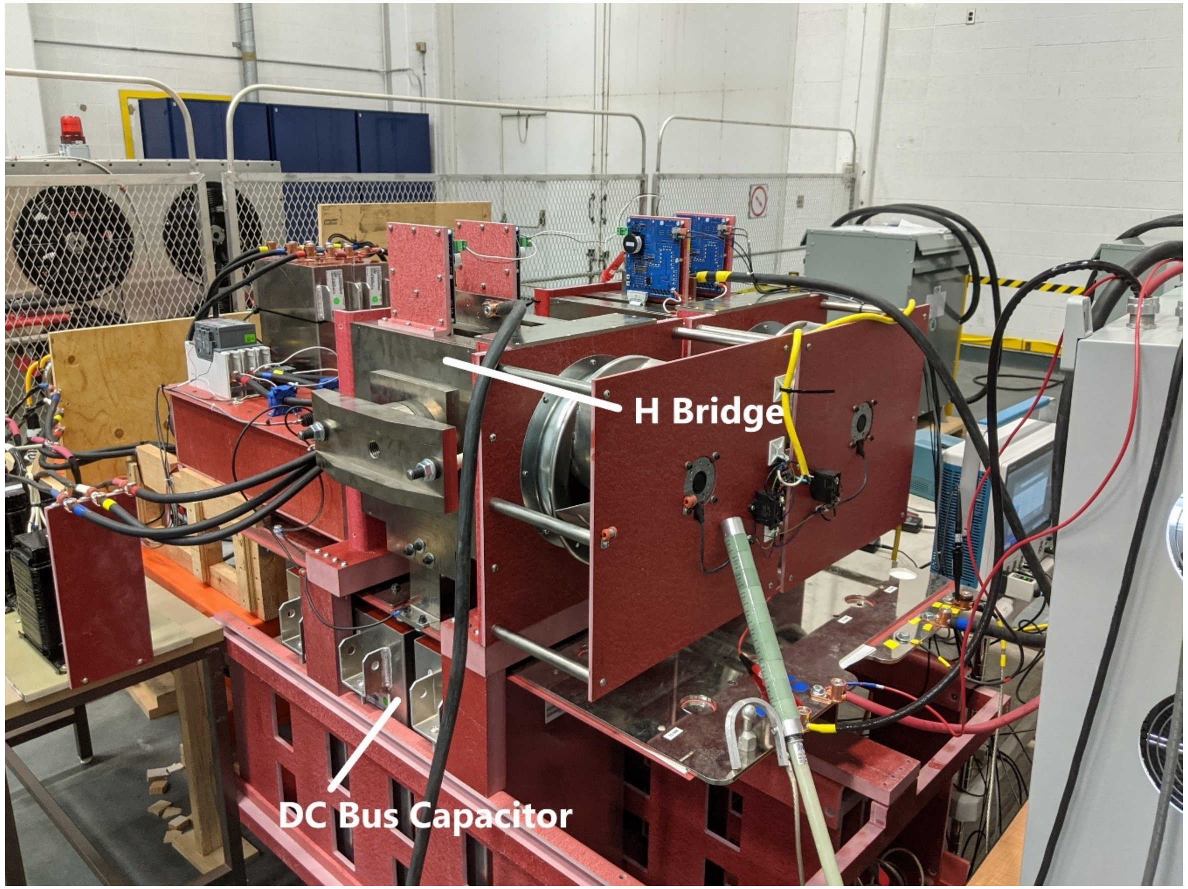



# Test results: experimental setup

- **Assembled 2-kV, 167-kVA module connected to 600 V grid through 600V/960V transformer**
- **Variable resistive load (20 to 80 Ohm) at the output of the H-bridge**
- **H-bridge switching frequency of 1 kHz**
- **Synthesized AC load voltage at 50 Hz**

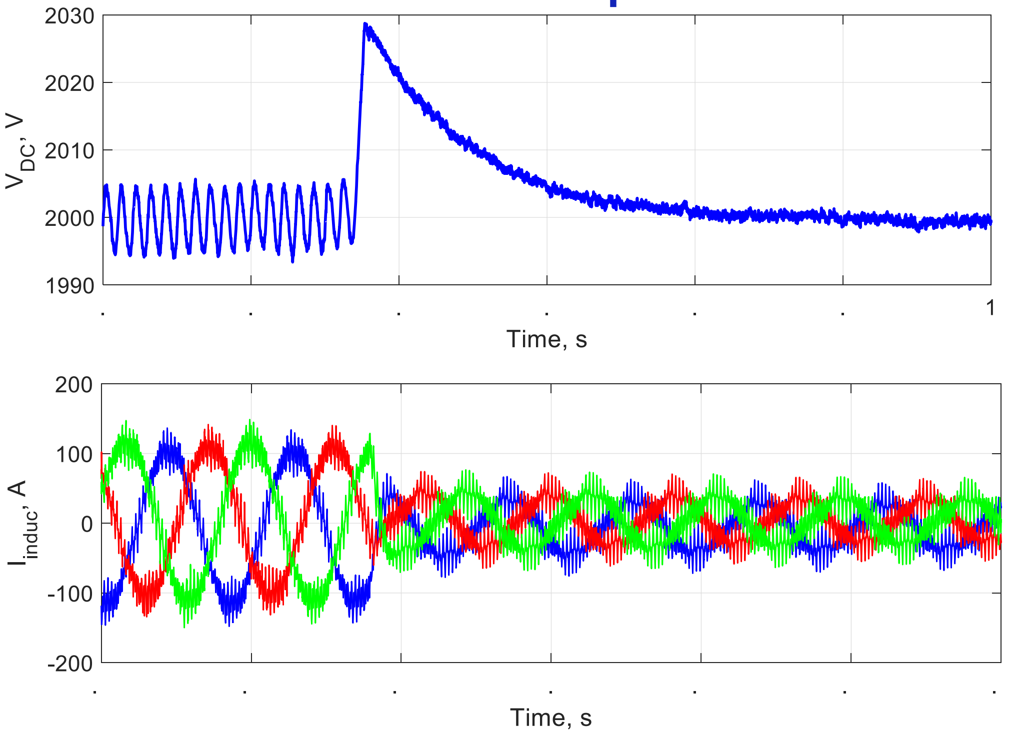
# Test results: experimental setup



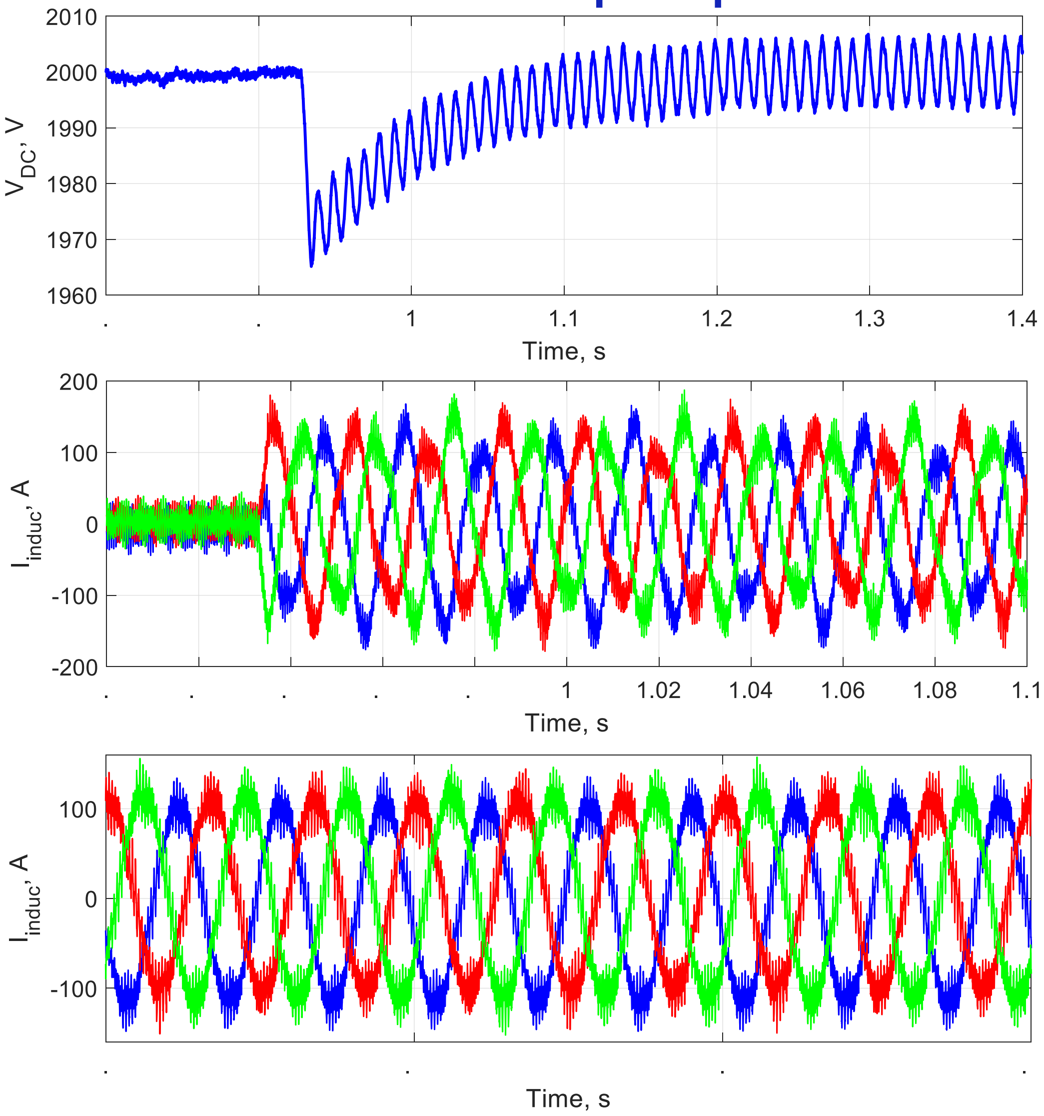



# Test results: experimental setup

## Load drop




## Load pickup



# Concluding remarks

- **Comprehensive validation of the proposed control strategy: offline simulations, real-time testing and experimental validation**
- **Optimal control design for a set of standard control problems in the application of grid-tied inverters**
  - Systematic design using powerful optimization tools (if reduced to a convex problem formulation)
  - Further developments may include model uncertainty, characterizing limits of performance, etc.
- **Many tools are available at IREQ to test new approaches**

# Concluding remarks

- **For further details, please see the following publication:**

**Rimorov, D., Tremblay, O., Slimani, K., Gagnon, R., & Couillard, B. (2022). Gain Scheduling Control Design for Active Front End for Power-Hardware-in-The-Loop Application: An LMI Approach. IEEE Transactions on Energy Conversion.**

- **Reach out to the SimP team for questions/discussions or if interested in collaboration!**
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# Appendix

## AFE parameters

| Description | Value |
|---|---|
| Nominal LL AC voltage, RMS, V | 960 |
| AFE nominal power, kVA | 167 |
| Nominal DC voltage, V | 2000 |
| AFE switching frequency, kHz | 2 |
| DC link capacitor, mF | 13.92 |
| AC output filter inductance, mH | 1.875 |
| AC output filter capacitance (Delta connected), uF | 66 |